TRANSMITTAL OF FORMAL DRAWINGS

Docket No.
BUR9-1999-0235-US1

In Re Application Of: **D. Hathaway**

Serial No.	Filing Date	Batch No.	Examiner	Art Unit
09/617,908	7/14/00			

Invention: **METHOD AND APPARATUS FOR MAKING INTEGRATED CIRCUITS HAVING GATED CLOCK TREES**

Address to
Assistant Commissioner for Patents
Washington, D.C. 20231

Transmitted herewith are:

29 sheets of formal drawing(s) for this application.

Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c) on the reverse side of the drawing.

Mark R Ferran
Signature

Dated: **12/7/00**

Mark R. Ferran
Reg. No. 46,695
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3 Lear Jet Lane, Suite 201
Latham, NY 12110
(518) 220-1850

I certify that this document and attached formal drawings are being deposited on **12/7/00** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Kim Dwileski
Signature of Person Mailing Correspondence

Kim Dwileski
Typed or Printed Name of Person Mailing Correspondence

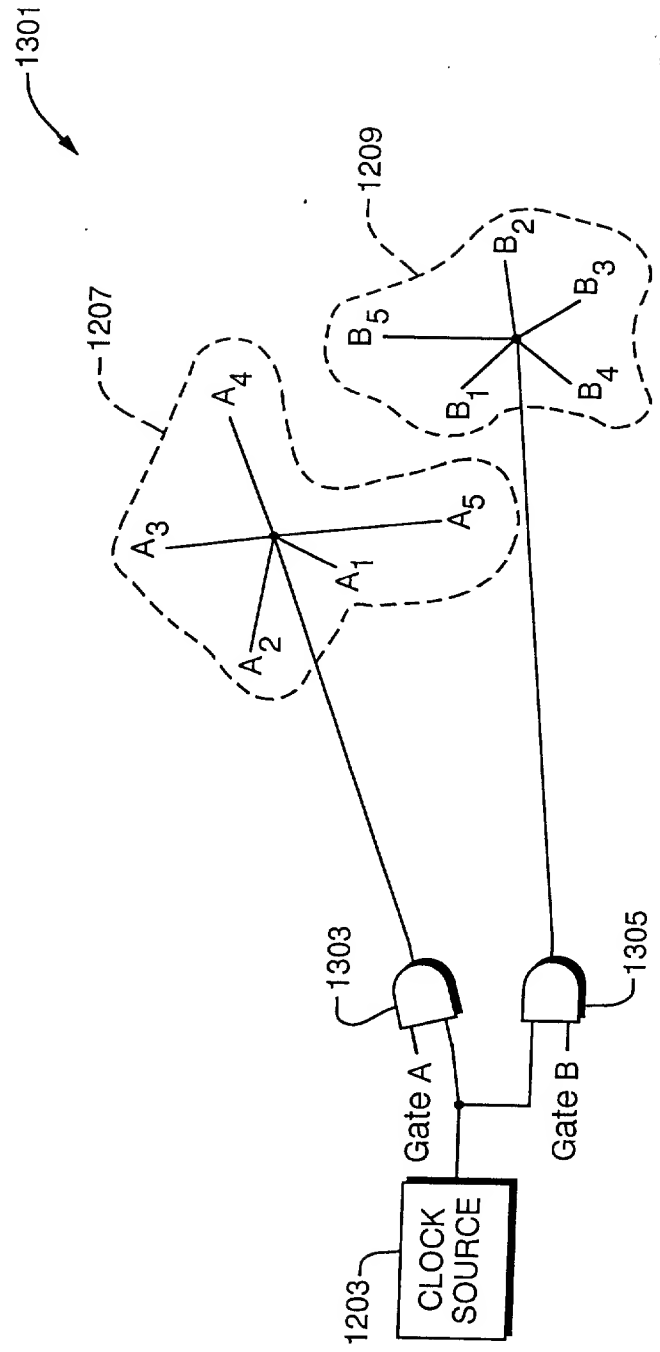

1301
1209
1207
B2
B3
B5
B1
B4
A4
A3
A5
A1
A2
1303
1305
Gate A
Gate B
CLOCK SOURCE
1203

FIG. 13

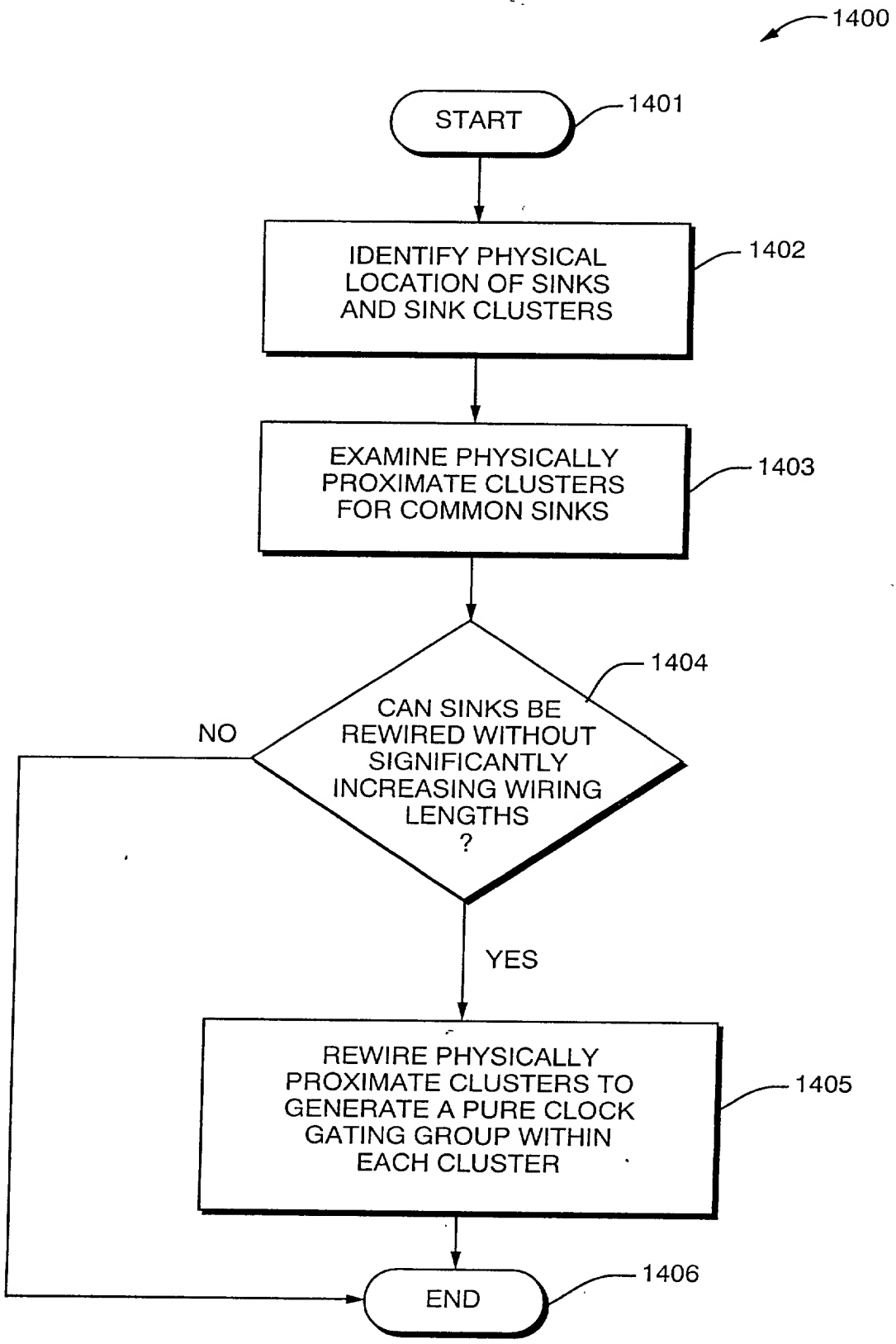

1400
START
1401
IDENTIFY PHYSICAL LOCATION OF SINKS AND SINK CLUSTERS
1402
EXAMINE PHYSICALLY PROXIMATE CLUSTERS FOR COMMON SINKS
1403
CAN SINKS BE REWIRED WITHOUT SIGNIFICANTLY INCREASING WIRING LENGTHS ?
1404
NO
YES
REWIRE PHYSICALLY PROXIMATE CLUSTERS TO GENERATE A PURE CLOCK GATING GROUP WITHIN EACH CLUSTER
1405
END
1406

FIG. 14

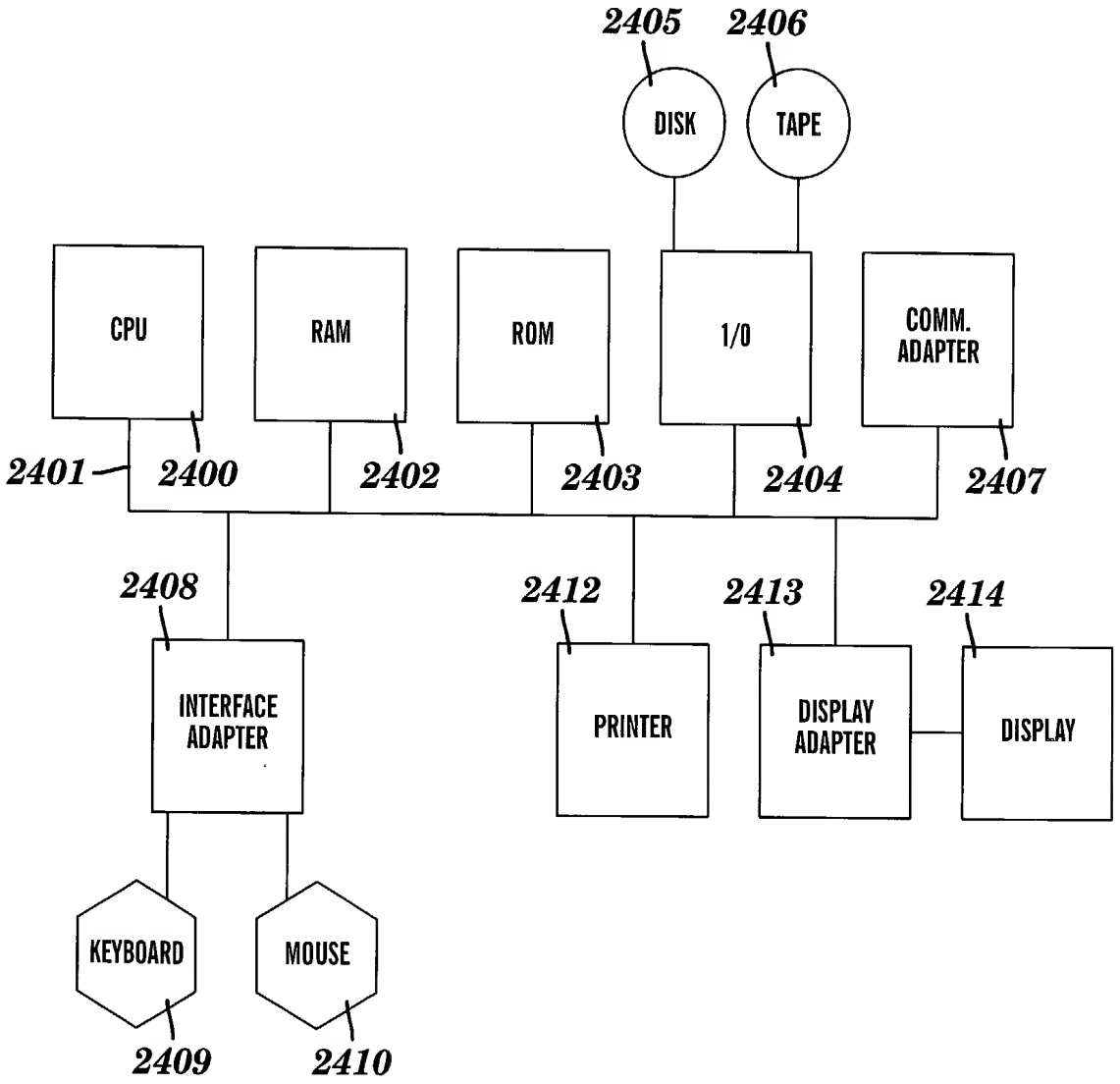

2405
2406
DISK
TAPE
CPU
RAM
ROM
1/0
COMM. ADAPTER
2401
2400
2402
2403
2404
2407
2408
2412
2413
2414
INTERFACE ADAPTER
PRINTER
DISPLAY ADAPTER
DISPLAY
KEYBOARD
MOUSE
2409
2410

FIG. 15

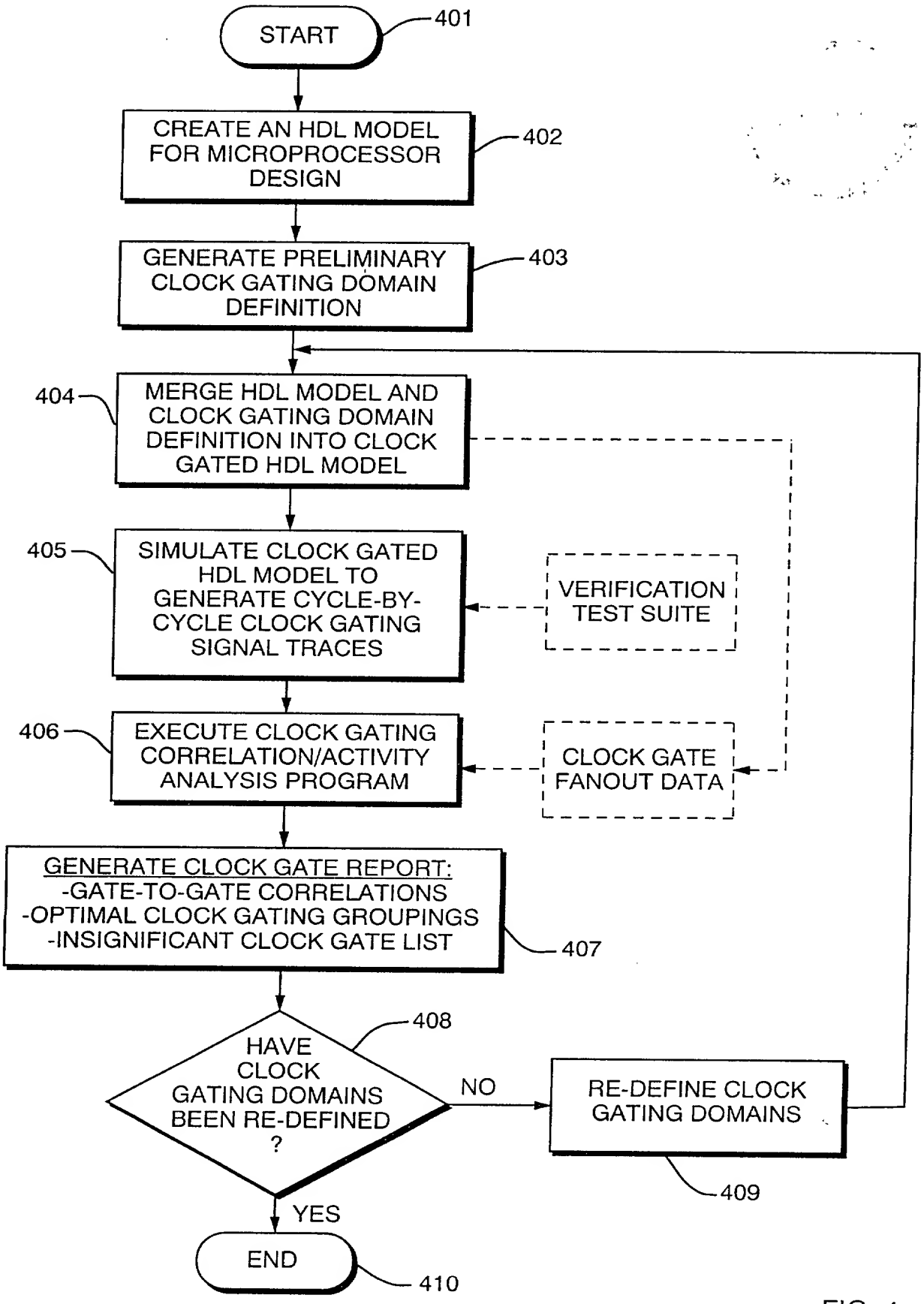

START
401
CREATE AN HDL MODEL FOR MICROPROCESSOR DESIGN
402
GENERATE PRELIMINARY CLOCK GATING DOMAIN DEFINITION
403
404
MERGE HDL MODEL AND CLOCK GATING DOMAIN DEFINITION INTO CLOCK GATED HDL MODEL
405
SIMULATE CLOCK GATED HDL MODEL TO GENERATE CYCLE-BY-CYCLE CLOCK GATING SIGNAL TRACES
VERIFICATION TEST SUITE
406
EXECUTE CLOCK GATING CORRELATION/ACTIVITY ANALYSIS PROGRAM
CLOCK GATE FANOUT DATA
GENERATE CLOCK GATE REPORT:
-GATE-TO-GATE CORRELATIONS
-OPTIMAL CLOCK GATING GROUPINGS
-INSIGNIFICANT CLOCK GATE LIST
407
408
HAVE CLOCK GATING DOMAINS BEEN RE-DEFINED ?
NO
RE-DEFINE CLOCK GATING DOMAINS
409
YES
END
410

FIG. 4

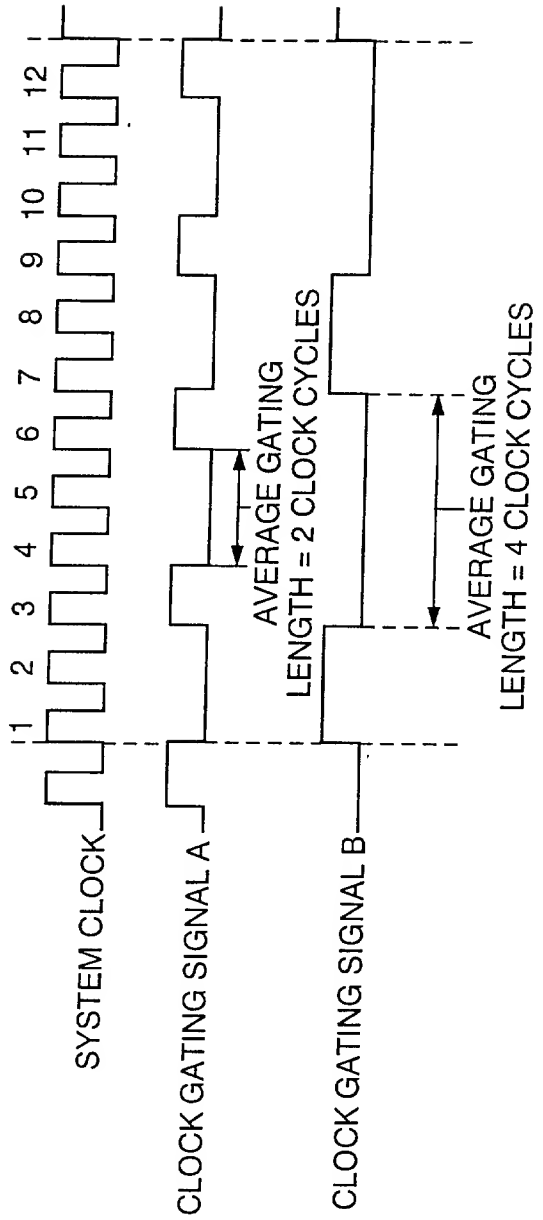
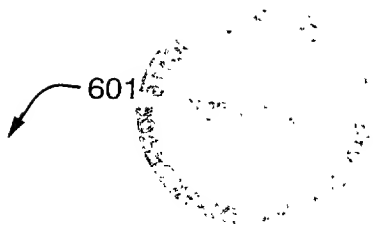

1
2
3
4
5
6
7
8
9
10
11
12
SYSTEM CLOCK
CLOCK GATING SIGNAL A
CLOCK GATING SIGNAL B
AVERAGE GATING
LENGTH = 2 CLOCK CYCLES
AVERAGE GATING
LENGTH = 4 CLOCK CYCLES

FIG. 5



ClockGate Analysis

603
Calculated number of clockgates: 3
57 Vectors analyzed
Writing activity file clock_groups.aet

605
ClockGate Report

Clock	Activity	%Latches	Usefullness ((1-activity) * (%Latches*100))
CLKG_A	0.316	0.40	27.4
CLKG_B	0.316	0.50	34.2
CLKG_C	0.947	0.10	0.5

Useless CLOCKGATES as defined by threshold: 5

Signal CLKG_C has a usefullness metric of 0.5

607
Writing Correlation File clock_groups.cor
Correlated CLOCKGATE Groups at threshold: 0.9
GROUP 1 Correlation=
CLKG_A : activity 0.316
CLKG_B : activity 0.316

CLOCK_GROUPS.COR file

Signal Correlation Report

	CLKG $\overline{A}$	CLKG $\overline{B}$	CLKG $\overline{C}$
CLKG_A	1.00	0.95	0.37
CLKG_B	0.95	1.00	0.37
CLKG_C	0.37	0.37	1.00

609

FIG. 6

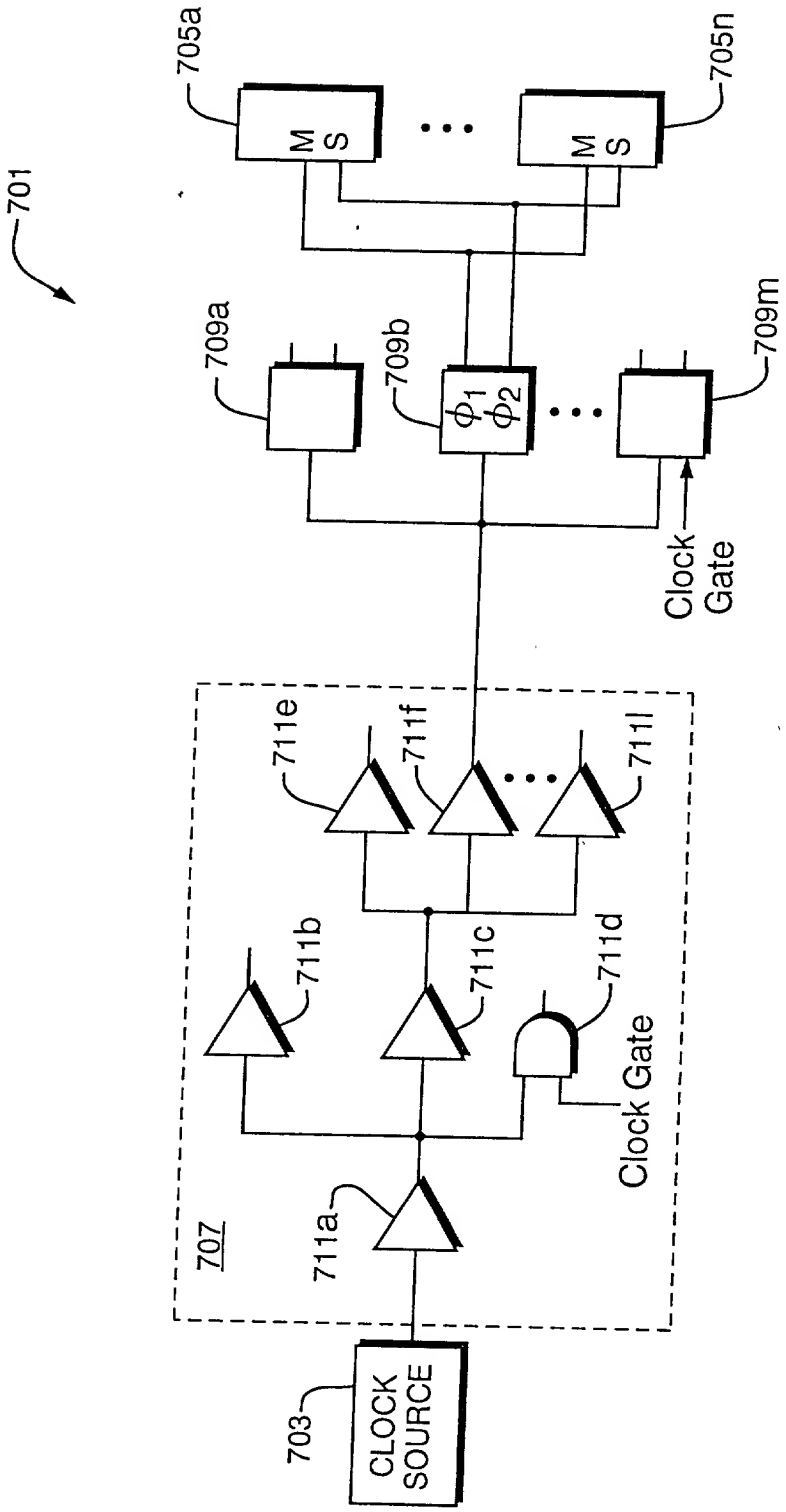

701
705a
705n
M
S
709a
709b
709m
ϕ_1
ϕ_2
Clock Gate
707
711a
711b
711c
711d
711e
711f
711l
Clock Gate
703
CLOCK SOURCE

FIG. 7

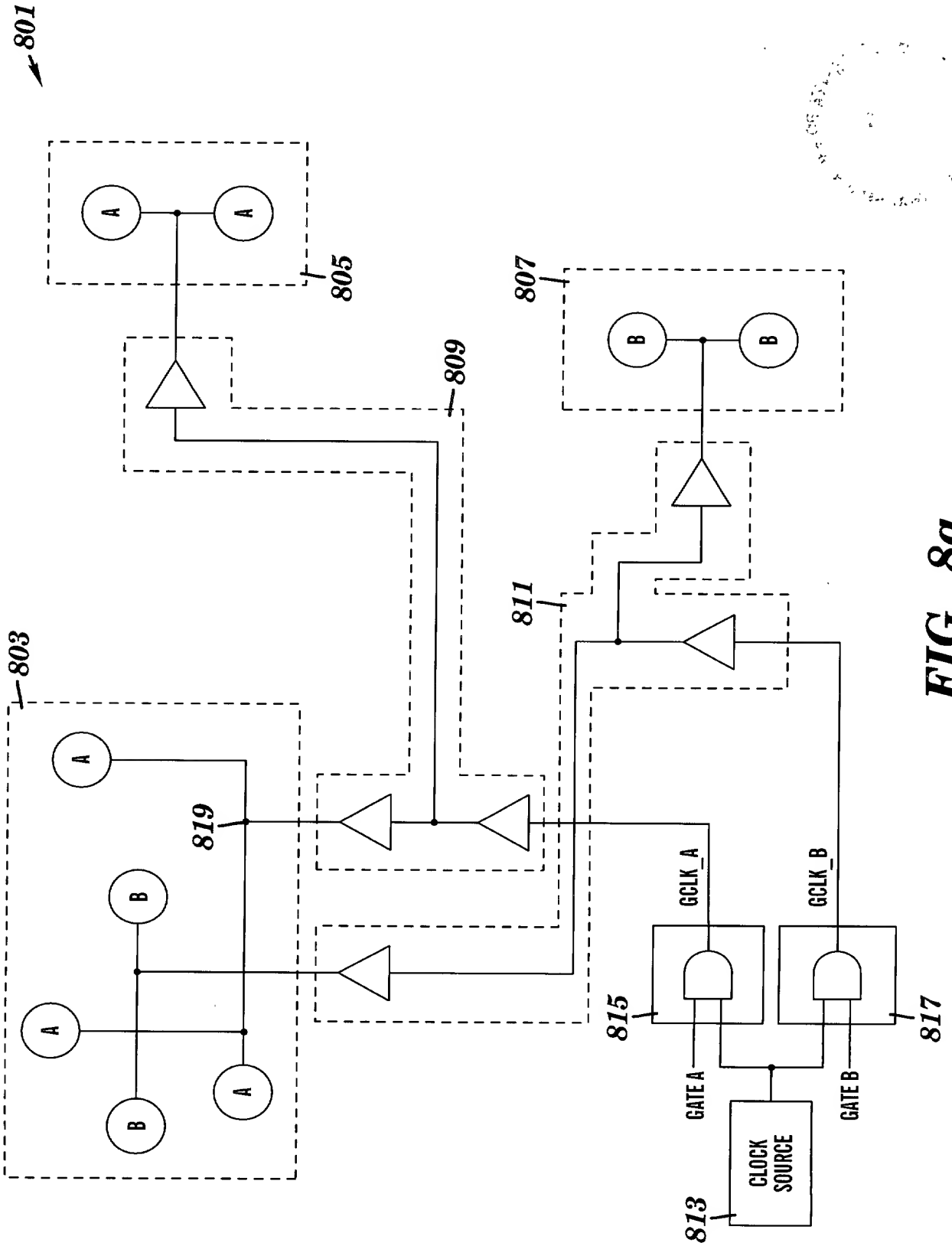

801
805
807
809
811
803
819
815
817
813
A
B
GCLK_A
GCLK_B
GATE A
GATE B
CLOCK SOURCE

FIG. 8a

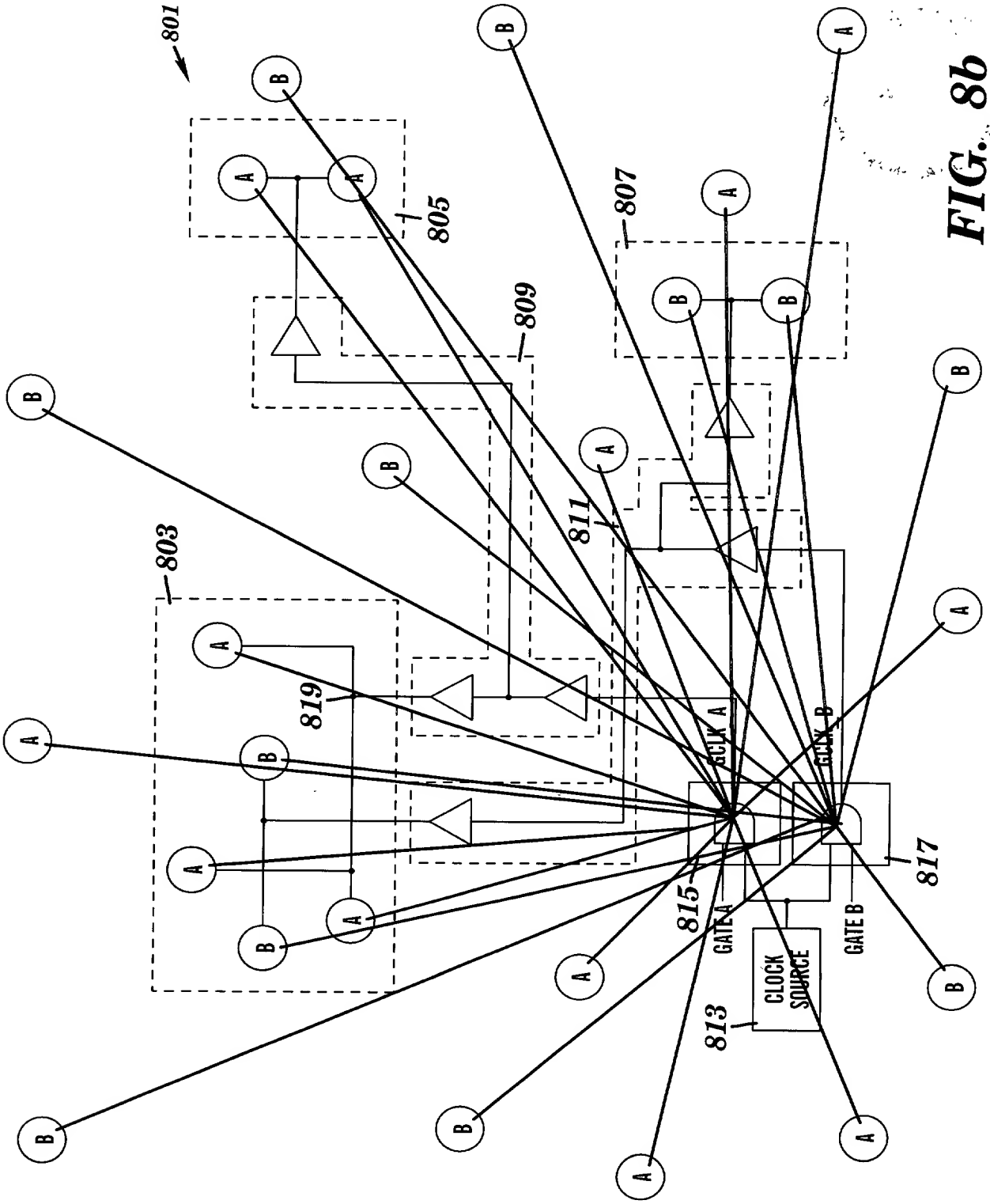

801
803
805
807
809
811
813
815
817
819
A
B
GCLK A
GCLK B
GATE A
GATE B
CLOCK SOURCE

FIG. 8b

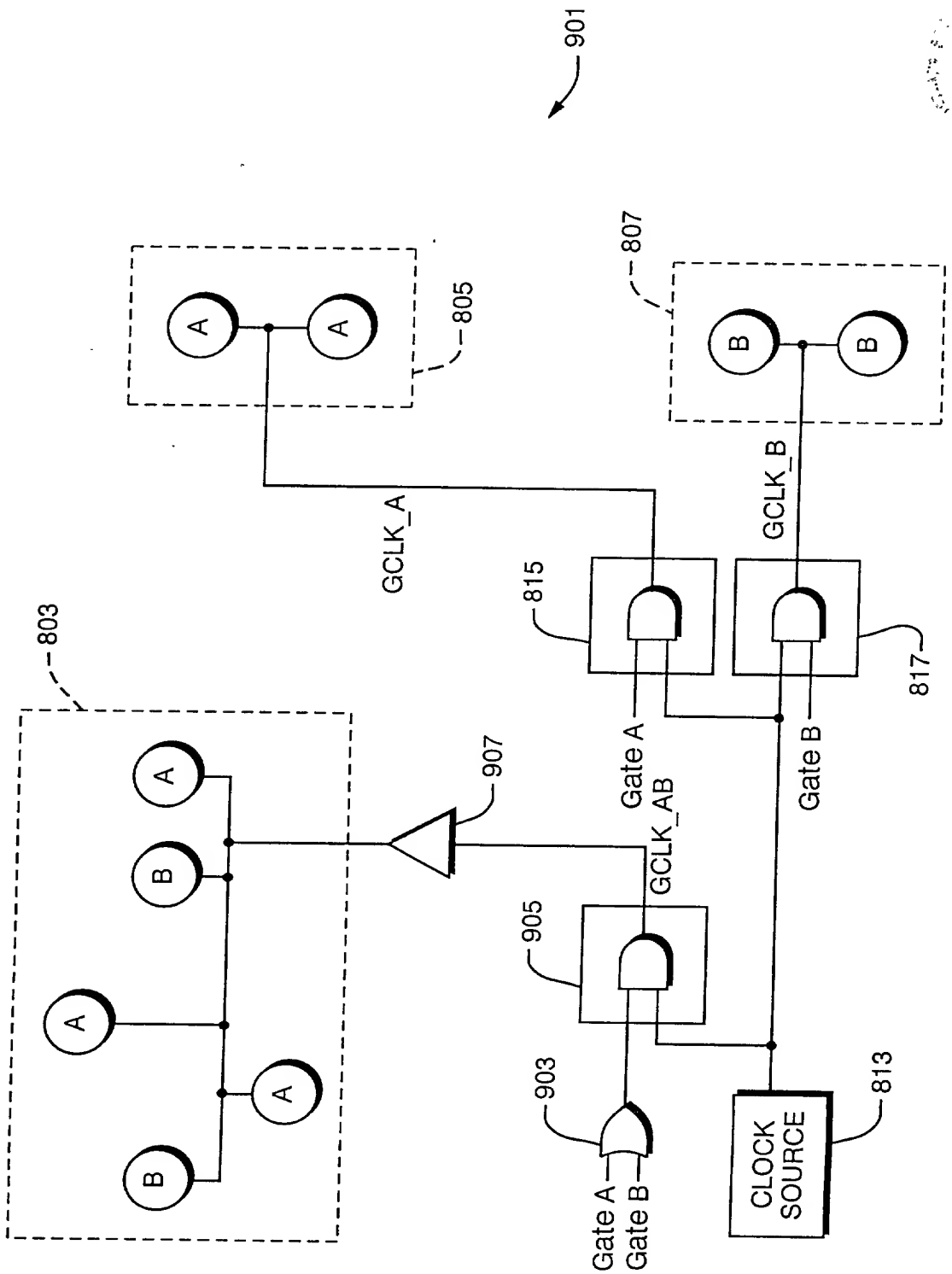

901
805
807
A
A
B
B
GCLK_A
GCLK_B
815
817
803
907
Gate A
Gate B
GCLK_AB
905
903
813
CLOCK SOURCE
Gate A
Gate B

FIG. 9

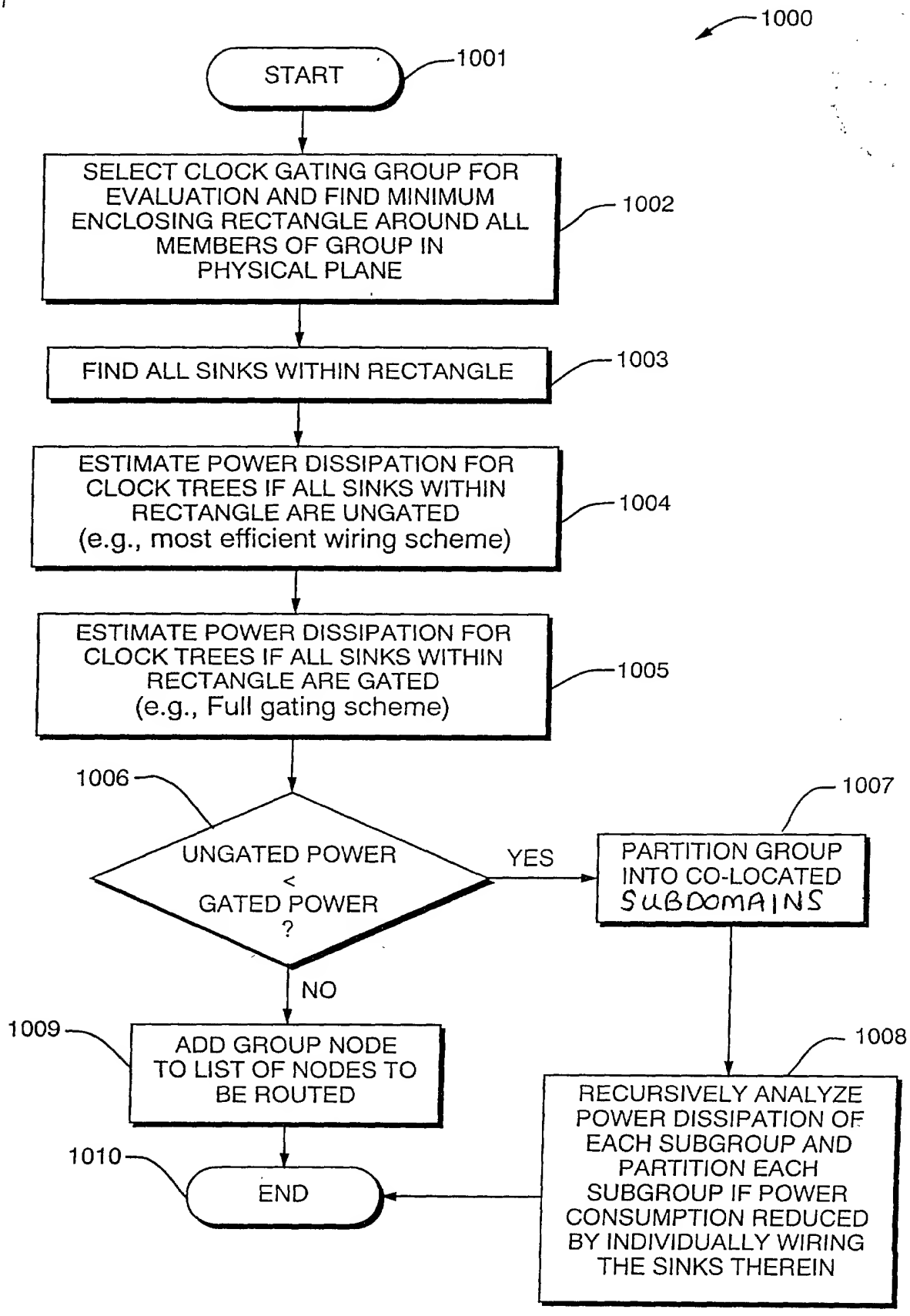

1000
START
1001
SELECT CLOCK GATING GROUP FOR EVALUATION AND FIND MINIMUM ENCLOSING RECTANGLE AROUND ALL MEMBERS OF GROUP IN PHYSICAL PLANE
1002
FIND ALL SINKS WITHIN RECTANGLE
1003
ESTIMATE POWER DISSIPATION FOR CLOCK TREES IF ALL SINKS WITHIN RECTANGLE ARE UNGATED (e.g., most efficient wiring scheme)
1004
ESTIMATE POWER DISSIPATION FOR CLOCK TREES IF ALL SINKS WITHIN RECTANGLE ARE GATED (e.g., Full gating scheme)
1005
1006
UNGATED POWER < GATED POWER ?
YES
1007
PARTITION GROUP INTO CO-LOCATED SUBDOMAINS
NO
1009
ADD GROUP NODE TO LIST OF NODES TO BE ROUTED
1008
RECURSIVELY ANALYZE POWER DISSIPATION OF EACH SUBGROUP AND PARTITION EACH SUBGROUP IF POWER CONSUMPTION REDUCED BY INDIVIDUALLY WIRING THE SINKS THEREIN
1010
END

FIG. 10

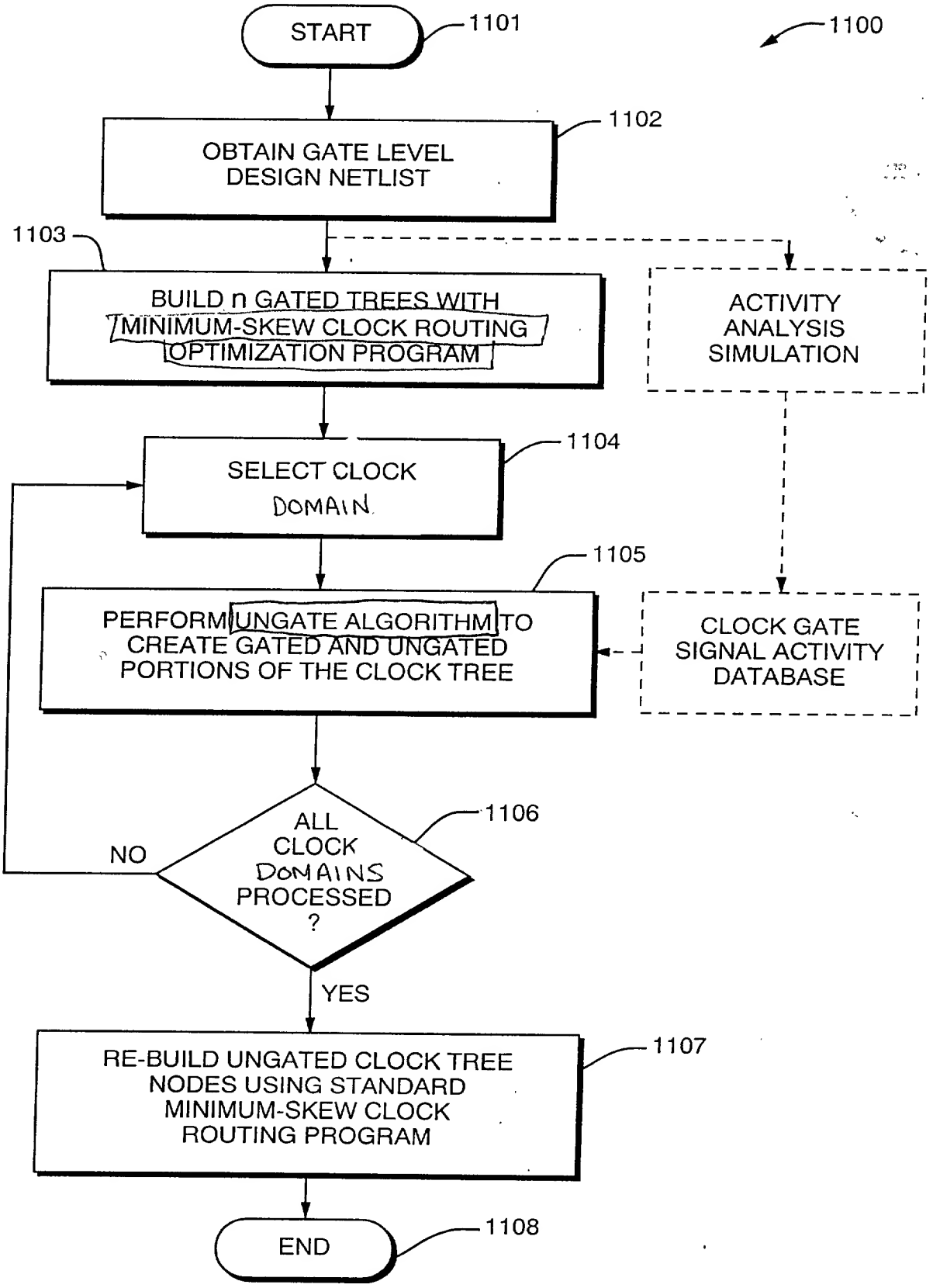

START
1101
1100
OBTAIN GATE LEVEL DESIGN NETLIST
1102
1103
BUILD n GATED TREES WITH MINIMUM-SKEW CLOCK ROUTING OPTIMIZATION PROGRAM
ACTIVITY ANALYSIS SIMULATION
SELECT CLOCK DOMAIN
1104
1105
PERFORM UNGATE ALGORITHM TO CREATE GATED AND UNGATED PORTIONS OF THE CLOCK TREE
CLOCK GATE SIGNAL ACTIVITY DATABASE
ALL CLOCK DOMAINS PROCESSED ?
1106
NO
YES
RE-BUILD UNGATED CLOCK TREE NODES USING STANDARD MINIMUM-SKEW CLOCK ROUTING PROGRAM
1107
END
1108

FIG. 11

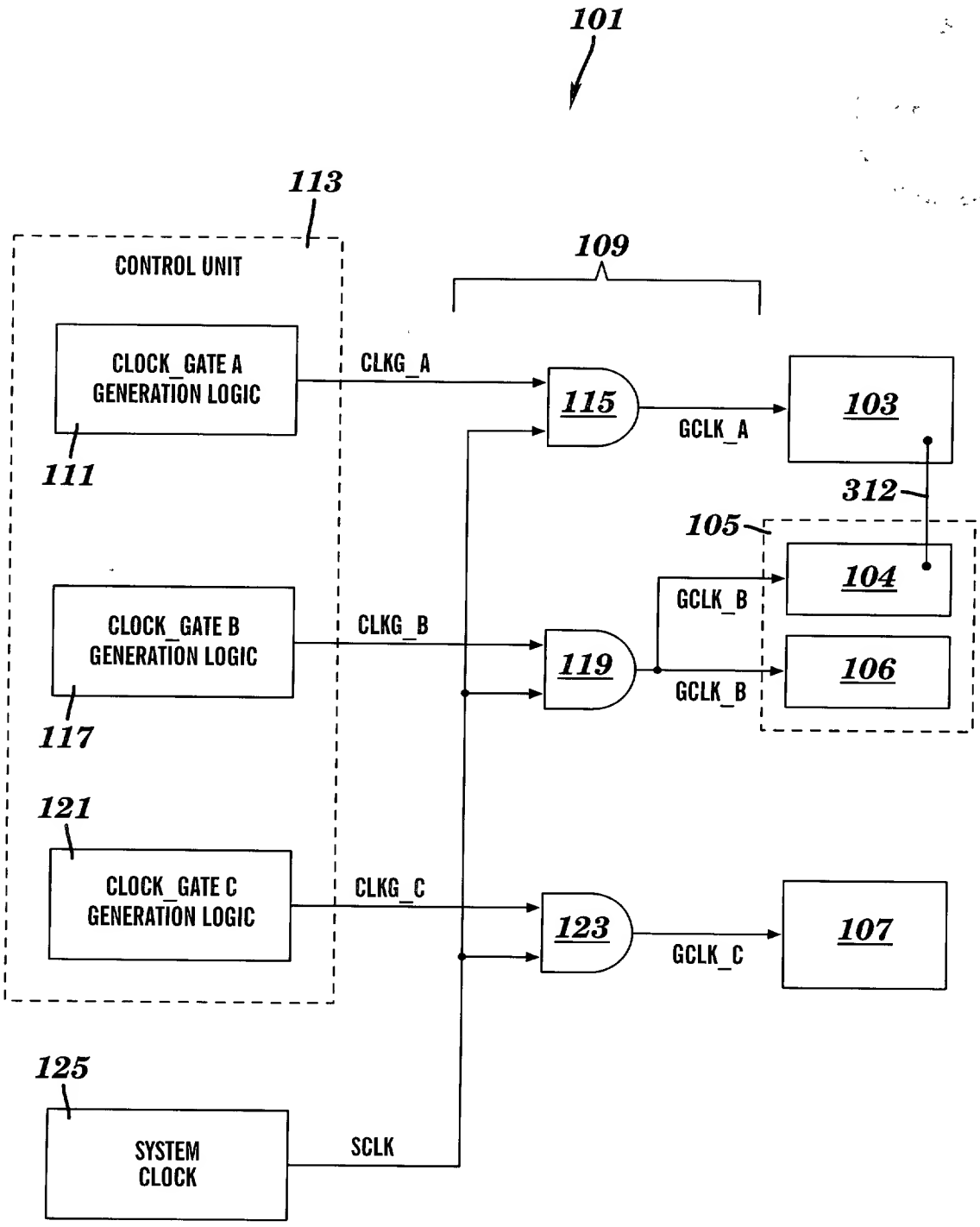

101
113
CONTROL UNIT
109
CLOCK_GATE A GENERATION LOGIC
CLKG_A
115
GCLK_A
103
111
312
105
104
CLOCK_GATE B GENERATION LOGIC
CLKG_B
GCLK_B
119
106
GCLK_B
117
121
CLOCK_GATE C GENERATION LOGIC
CLKG_C
123
GCLK_C
107
125
SYSTEM CLOCK
SCLK

FIG. 3b

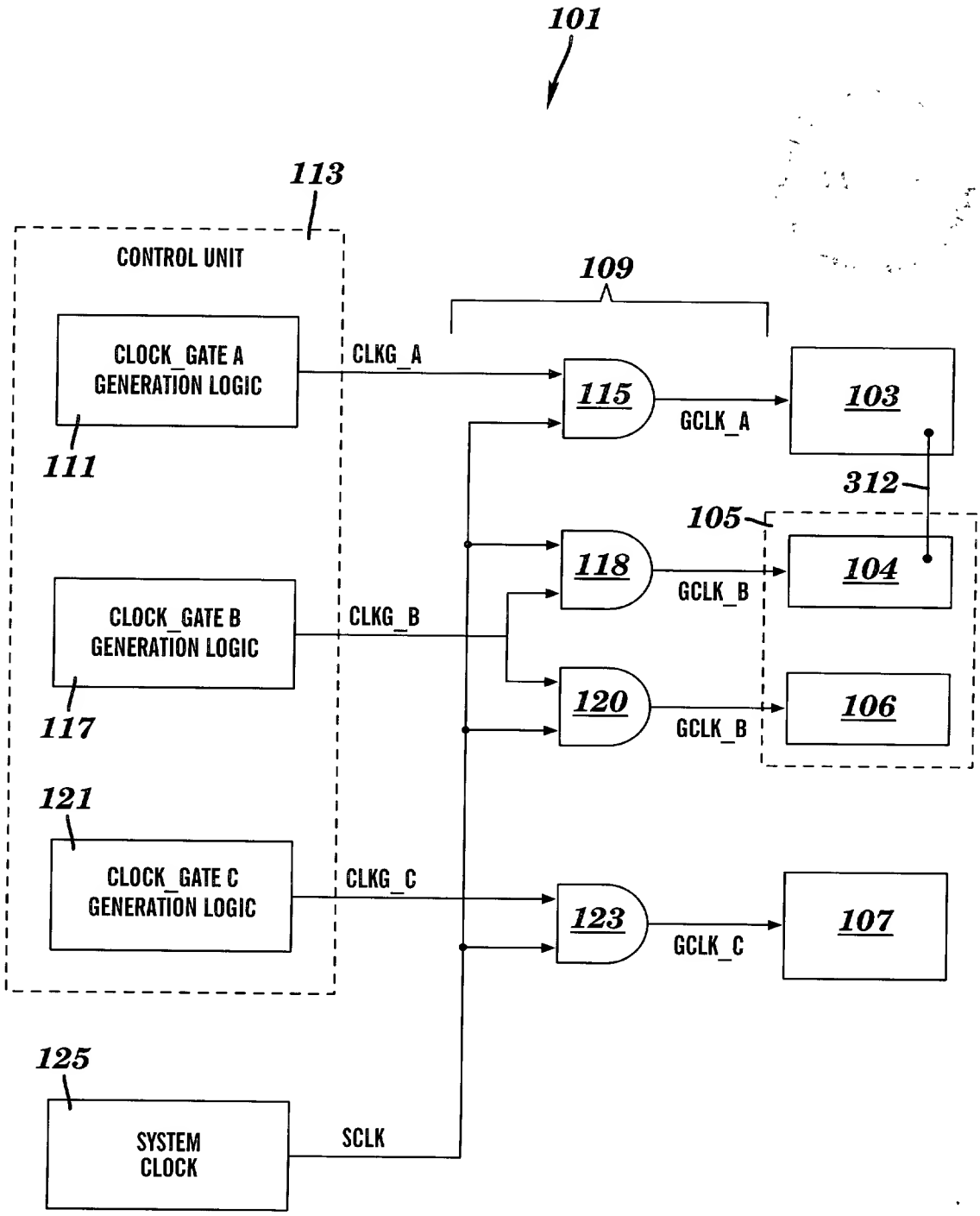

101
113
CONTROL UNIT
109
CLOCK_GATE A GENERATION LOGIC
CLKG_A
115
GCLK_A
103
111
312
105
118
GCLK_B
104
CLOCK_GATE B GENERATION LOGIC
CLKG_B
120
GCLK_B
106
117
121
CLOCK_GATE C GENERATION LOGIC
CLKG_C
123
GCLK_C
107
125
SYSTEM CLOCK
SCLK

FIG. 3c

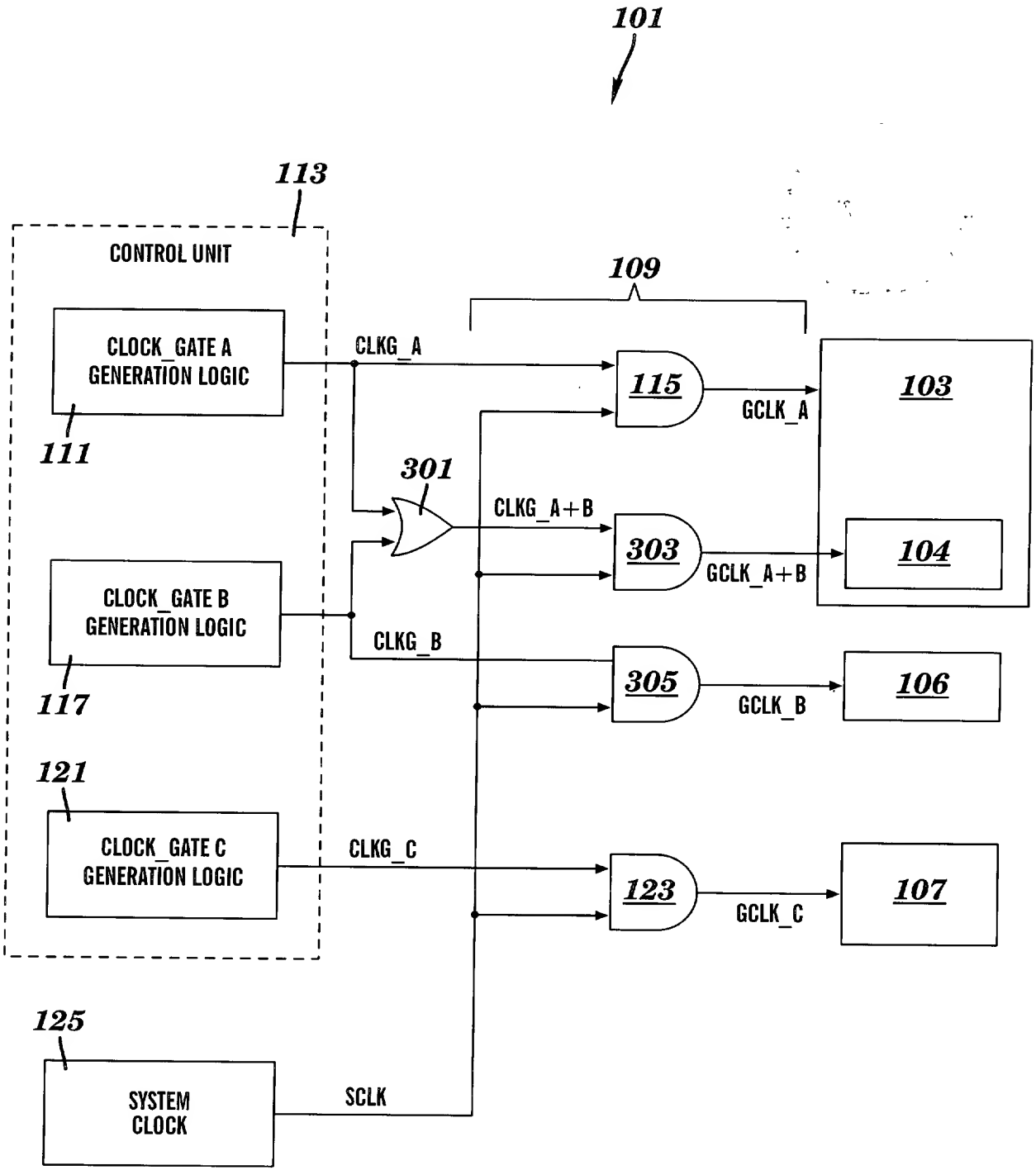

101
113
CONTROL UNIT
109
CLOCK_GATE A GENERATION LOGIC
111
CLKG_A
115
GCLK_A
103
301
CLKG_A+B
303
GCLK_A+B
104
CLOCK_GATE B GENERATION LOGIC
117
CLKG_B
305
GCLK_B
106
121
CLOCK_GATE C GENERATION LOGIC
CLKG_C
123
GCLK_C
107
125
SYSTEM CLOCK
SCLK

FIG. 3d

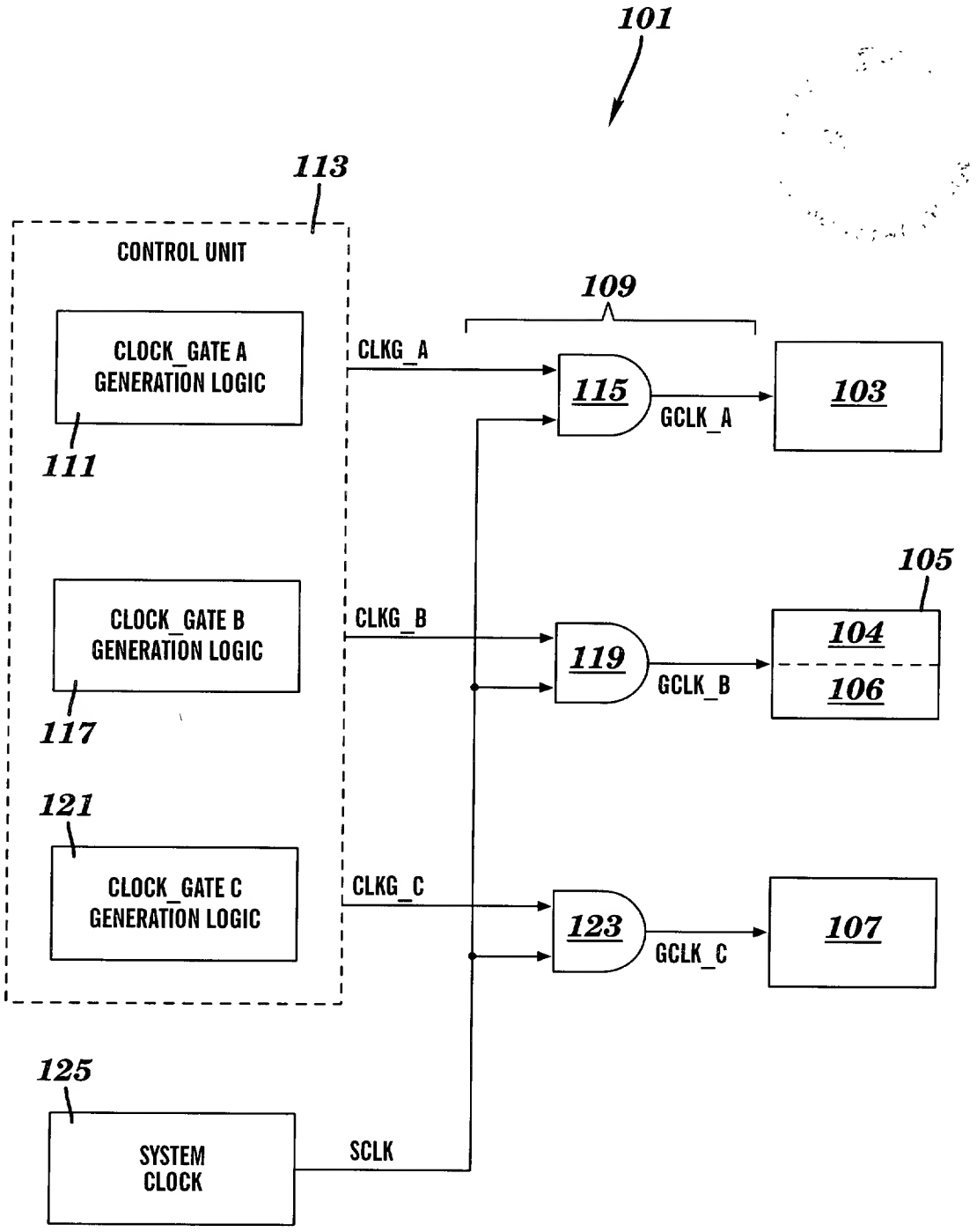

101
113
CONTROL UNIT
109
CLOCK_GATE A GENERATION LOGIC
111
CLKG_A
115
GCLK_A
103
CLOCK_GATE B GENERATION LOGIC
117
CLKG_B
119
GCLK_B
105
104
106
121
CLOCK_GATE C GENERATION LOGIC
CLKG_C
123
GCLK_C
107
125
SYSTEM CLOCK
SCLK

FIG. 1a

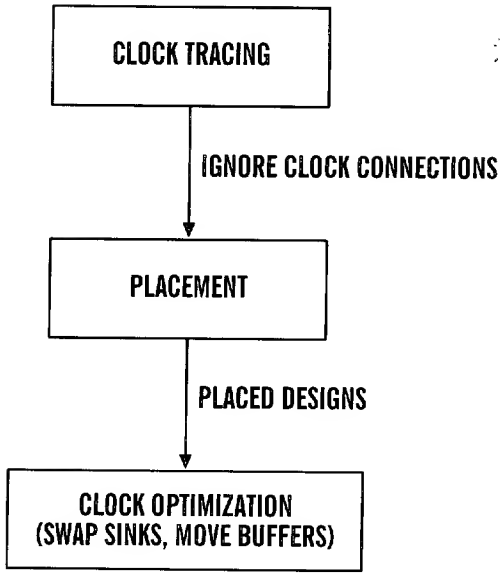

CLOCK TRACING
IGNORE CLOCK CONNECTIONS
PLACEMENT
PLACED DESIGNS
CLOCK OPTIMIZATION
(SWAP SINKS, MOVE BUFFERS)

FIG. 1b

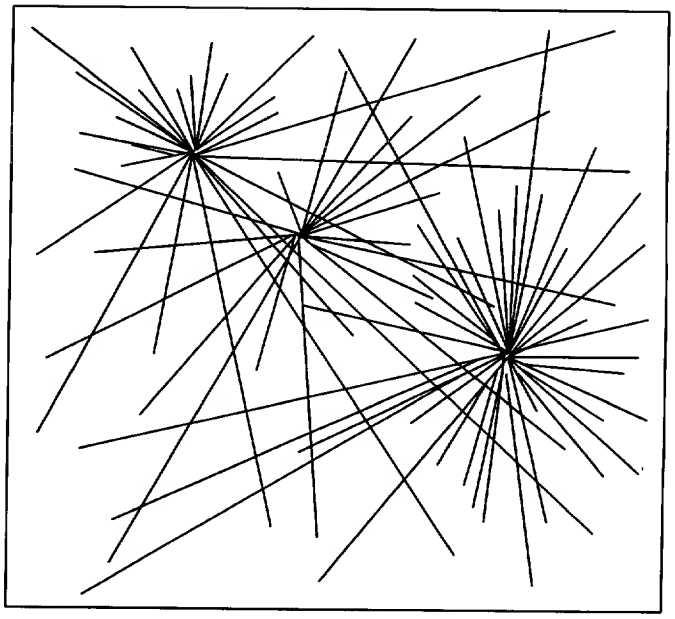


FIG. 1c

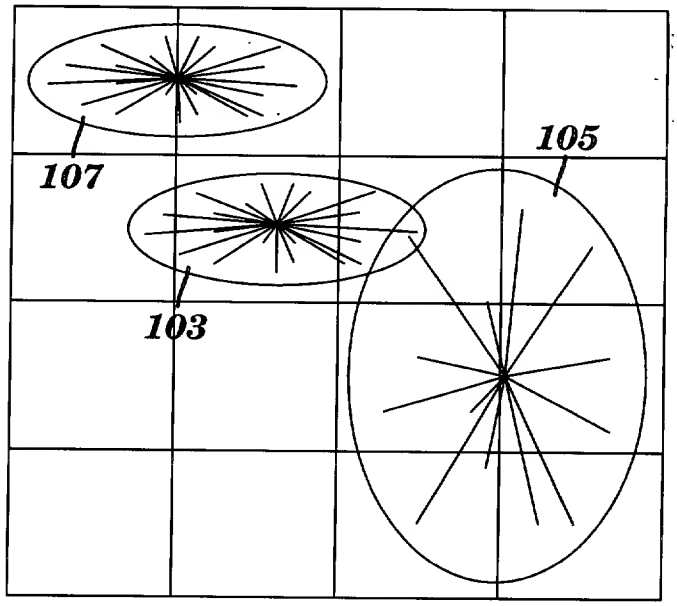


FIG. 2a-i

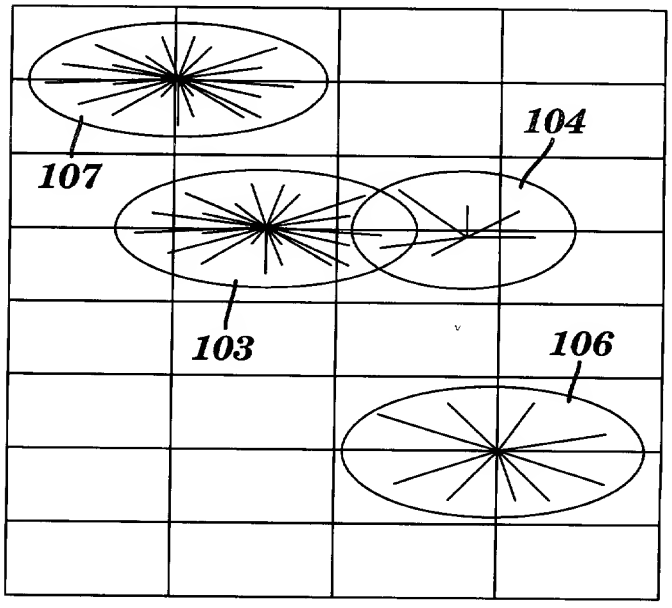


FIG. 2a-ii

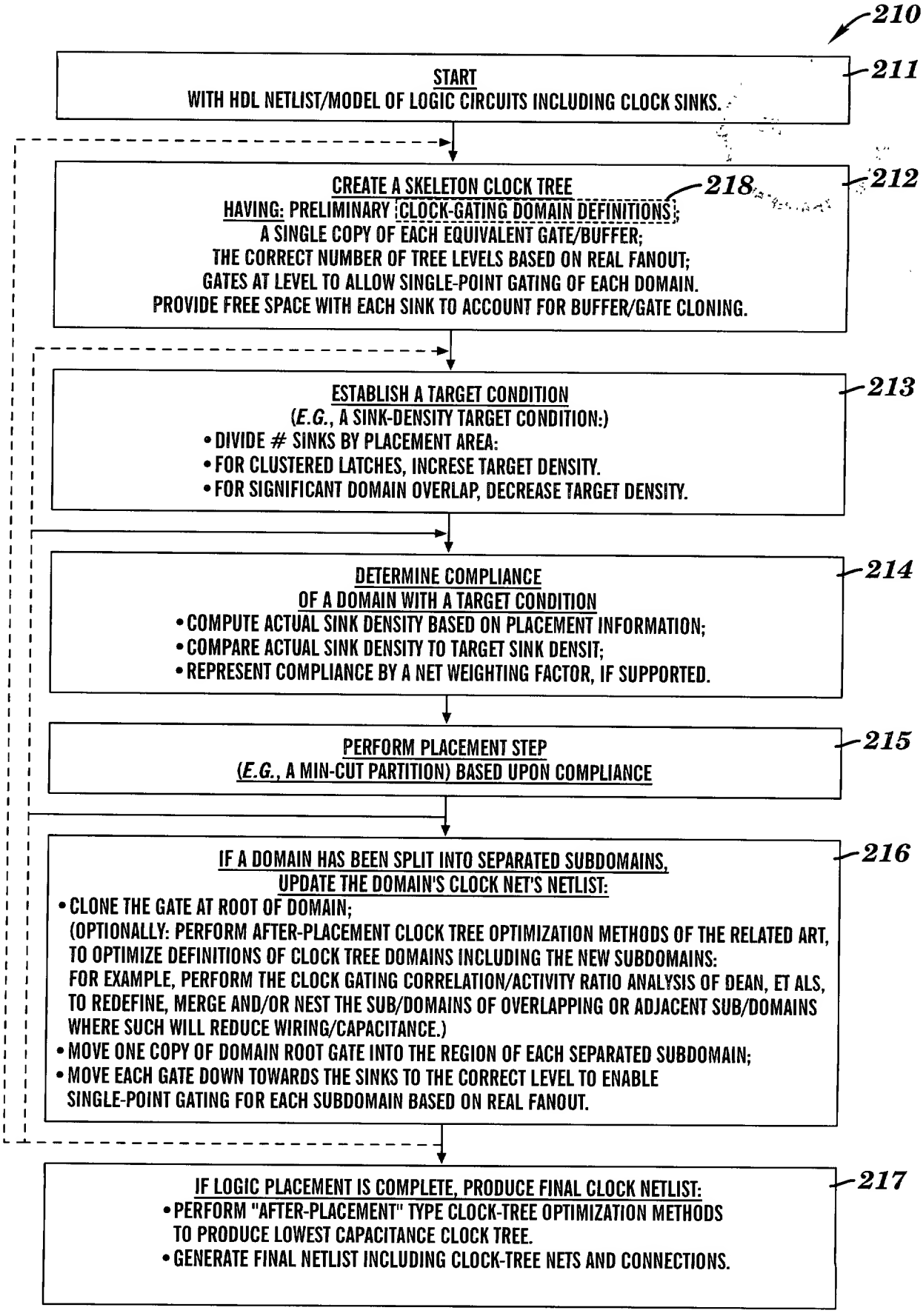

210
START
WITH HDL NETLIST/MODEL OF LOGIC CIRCUITS INCLUDING CLOCK SINKS.
211
CREATE A SKELETON CLOCK TREE
HAVING: PRELIMINARY CLOCK-GATING DOMAIN DEFINITIONS;
218
A SINGLE COPY OF EACH EQUIVALENT GATE/BUFFER;
THE CORRECT NUMBER OF TREE LEVELS BASED ON REAL FANOUT;
GATES AT LEVEL TO ALLOW SINGLE-POINT GATING OF EACH DOMAIN.
PROVIDE FREE SPACE WITH EACH SINK TO ACCOUNT FOR BUFFER/GATE CLONING.
212
ESTABLISH A TARGET CONDITION
(E.G., A SINK-DENSITY TARGET CONDITION:)
• DIVIDE # SINKS BY PLACEMENT AREA:
• FOR CLUSTERED LATCHES, INCRESE TARGET DENSITY.
• FOR SIGNIFICANT DOMAIN OVERLAP, DECREASE TARGET DENSITY.
213
DETERMINE COMPLIANCE
OF A DOMAIN WITH A TARGET CONDITION
• COMPUTE ACTUAL SINK DENSITY BASED ON PLACEMENT INFORMATION;
• COMPARE ACTUAL SINK DENSITY TO TARGET SINK DENSIT;
• REPRESENT COMPLIANCE BY A NET WEIGHTING FACTOR, IF SUPPORTED.
214
PERFORM PLACEMENT STEP
(E.G., A MIN-CUT PARTITION) BASED UPON COMPLIANCE
215
IF A DOMAIN HAS BEEN SPLIT INTO SEPARATED SUBDOMAINS,
UPDATE THE DOMAIN'S CLOCK NET'S NETLIST:
• CLONE THE GATE AT ROOT OF DOMAIN;
(OPTIONALLY: PERFORM AFTER-PLACEMENT CLOCK TREE OPTIMIZATION METHODS OF THE RELATED ART, TO OPTIMIZE DEFINITIONS OF CLOCK TREE DOMAINS INCLUDING THE NEW SUBDOMAINS:
FOR EXAMPLE, PERFORM THE CLOCK GATING CORRELATION/ACTIVITY RATIO ANALYSIS OF DEAN, ET ALS, TO REDEFINE, MERGE AND/OR NEST THE SUB/DOMAINS OF OVERLAPPING OR ADJACENT SUB/DOMAINS WHERE SUCH WILL REDUCE WIRING/CAPACITANCE.)
• MOVE ONE COPY OF DOMAIN ROOT GATE INTO THE REGION OF EACH SEPARATED SUBDOMAIN;
• MOVE EACH GATE DOWN TOWARDS THE SINKS TO THE CORRECT LEVEL TO ENABLE SINGLE-POINT GATING FOR EACH SUBDOMAIN BASED ON REAL FANOUT.
216
IF LOGIC PLACEMENT IS COMPLETE, PRODUCE FINAL CLOCK NETLIST:
• PERFORM "AFTER-PLACEMENT" TYPE CLOCK-TREE OPTIMIZATION METHODS TO PRODUCE LOWEST CAPACITANCE CLOCK TREE.
• GENERATE FINAL NETLIST INCLUDING CLOCK-TREE NETS AND CONNECTIONS.
217

FIG. 2b

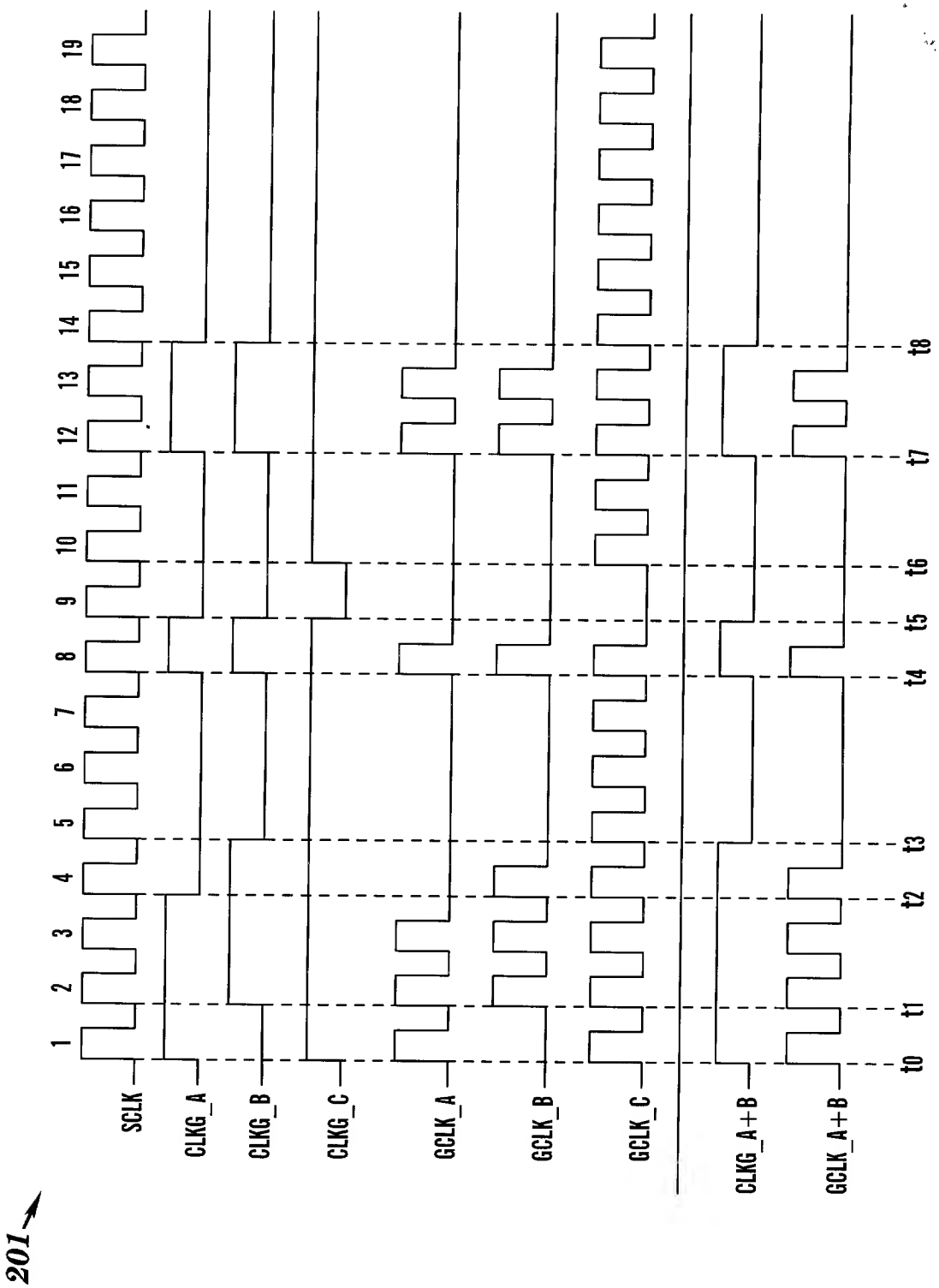

201
SCLK
CLKG_A
CLKG_B
CLKG_C
GCLK_A
GCLK_B
GCLK_C
CLKG_A+B
GCLK_A+B
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
t0
t1
t2
t3
t4
t5
t6
t7
t8

FIG. 2c

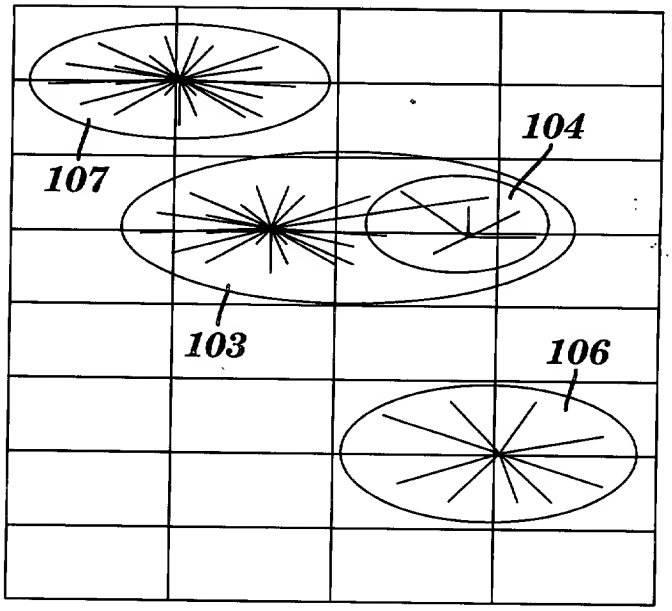


FIG. 2d

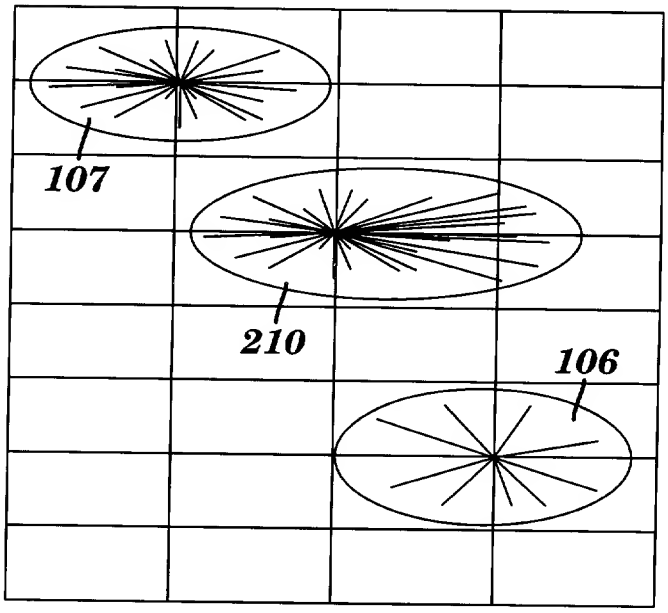


FIG. 2e

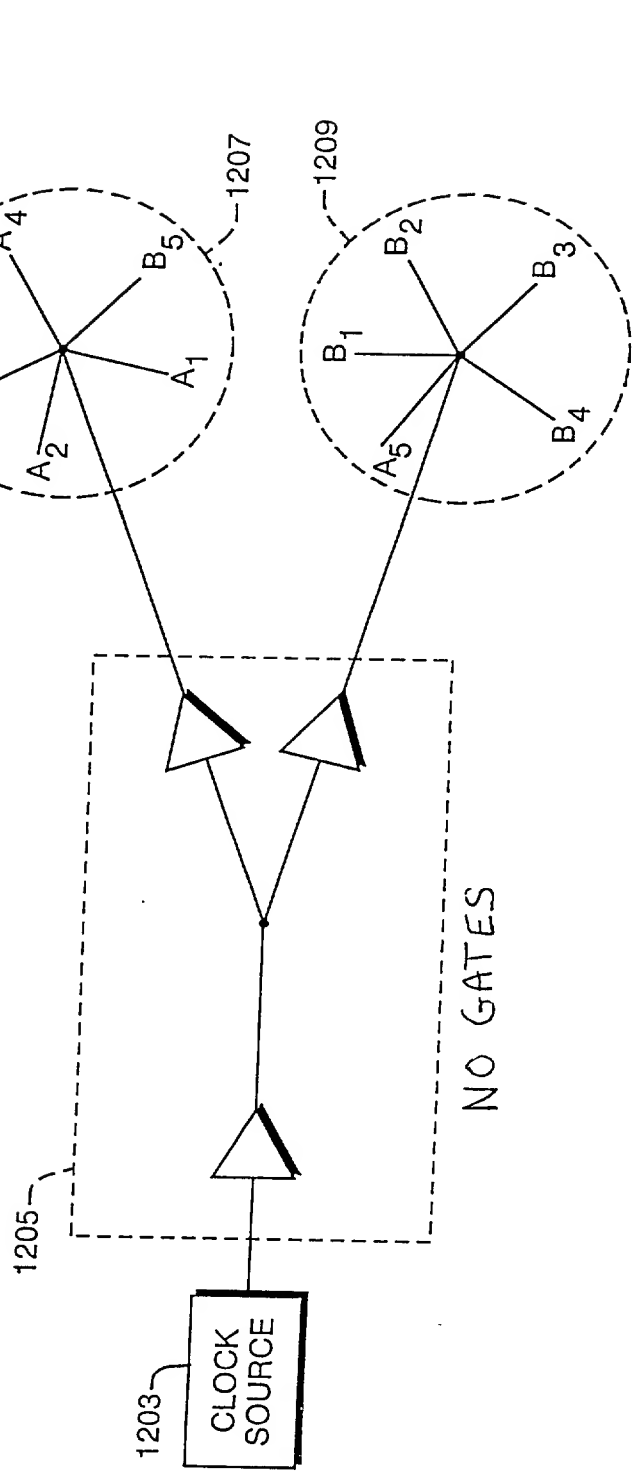

1201
1207
1209
A4
B5
A3
A1
A2
B2
B3
B1
B4
A5
1205
NO GATES
1203
CLOCK SOURCE

FIG. 12

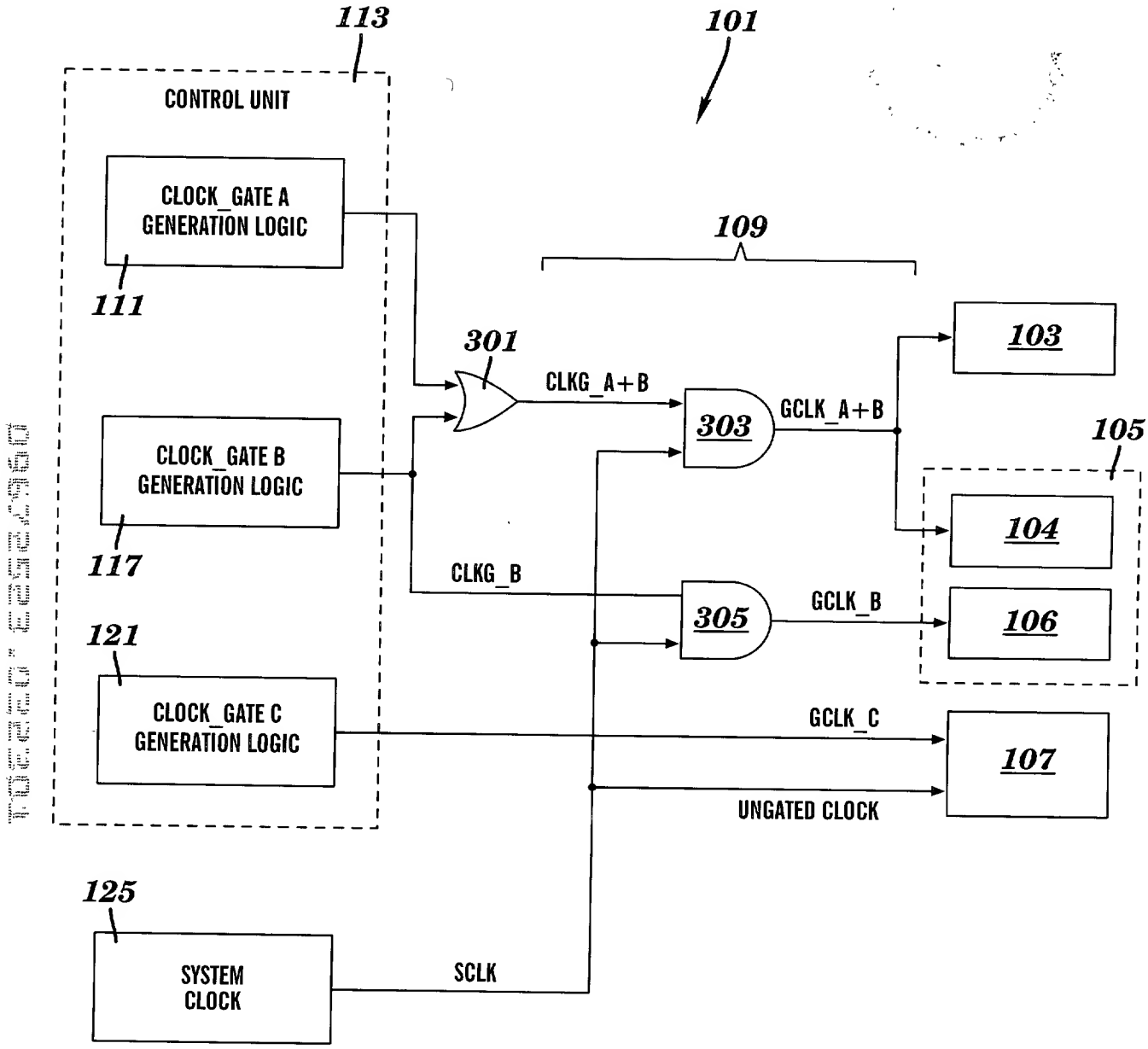

113
101
CONTROL UNIT
CLOCK_GATE A GENERATION LOGIC
111
109
301
CLKG_A+B
303
GCLK_A+B
103
105
CLOCK_GATE B GENERATION LOGIC
117
104
CLKG_B
305
GCLK_B
106
121
CLOCK_GATE C GENERATION LOGIC
GCLK_C
107
UNGATED CLOCK
125
SYSTEM CLOCK
SCLK

FIG. 3e

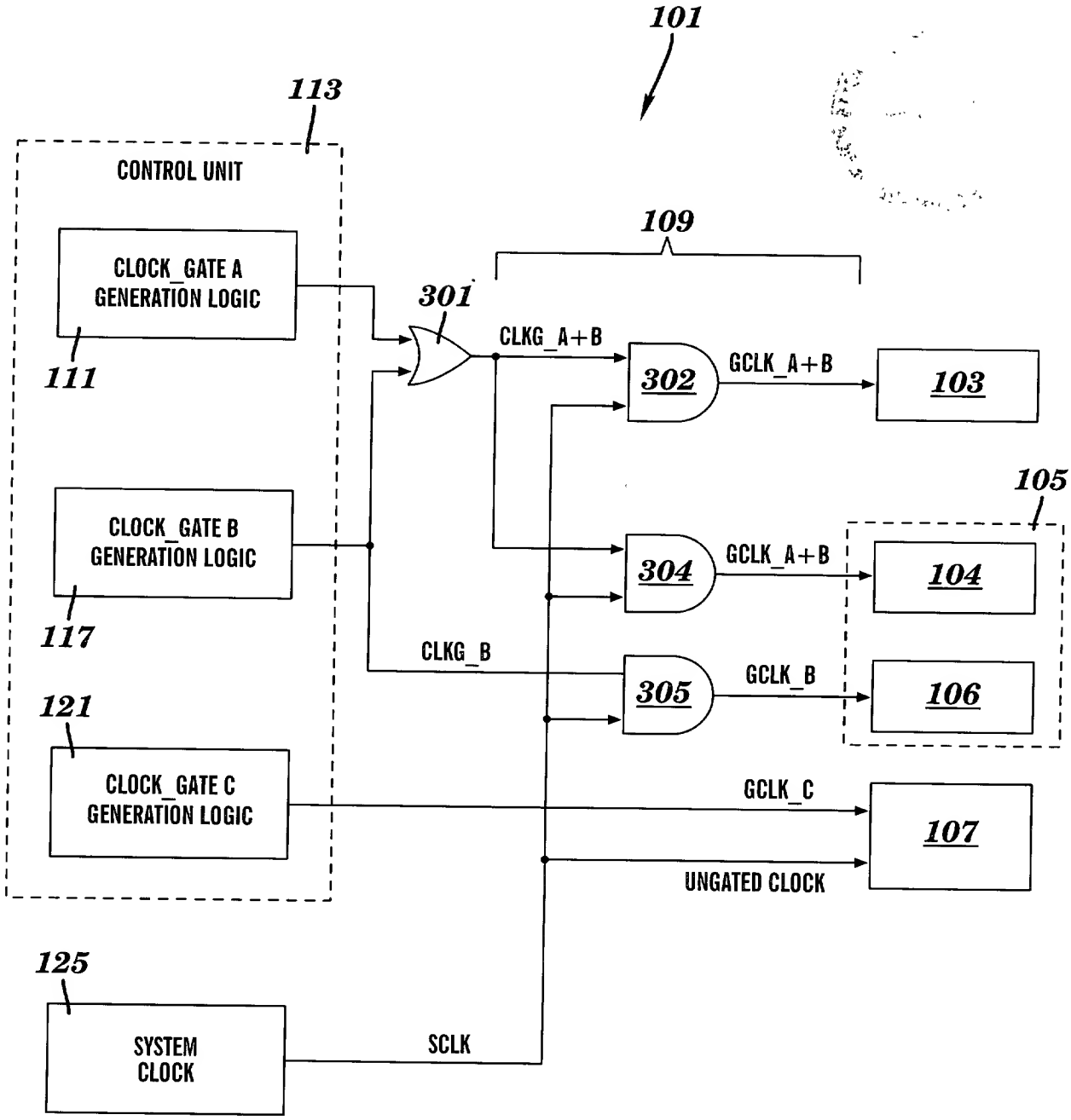

101
113
CONTROL UNIT
CLOCK_GATE A GENERATION LOGIC
111
CLOCK_GATE B GENERATION LOGIC
117
121
CLOCK_GATE C GENERATION LOGIC
125
SYSTEM CLOCK
SCLK
109
301
CLKG_A+B
302
GCLK_A+B
103
105
304
GCLK_A+B
104
CLKG_B
305
GCLK_B
106
GCLK_C
107
UNGATED CLOCK

FIG. 3f

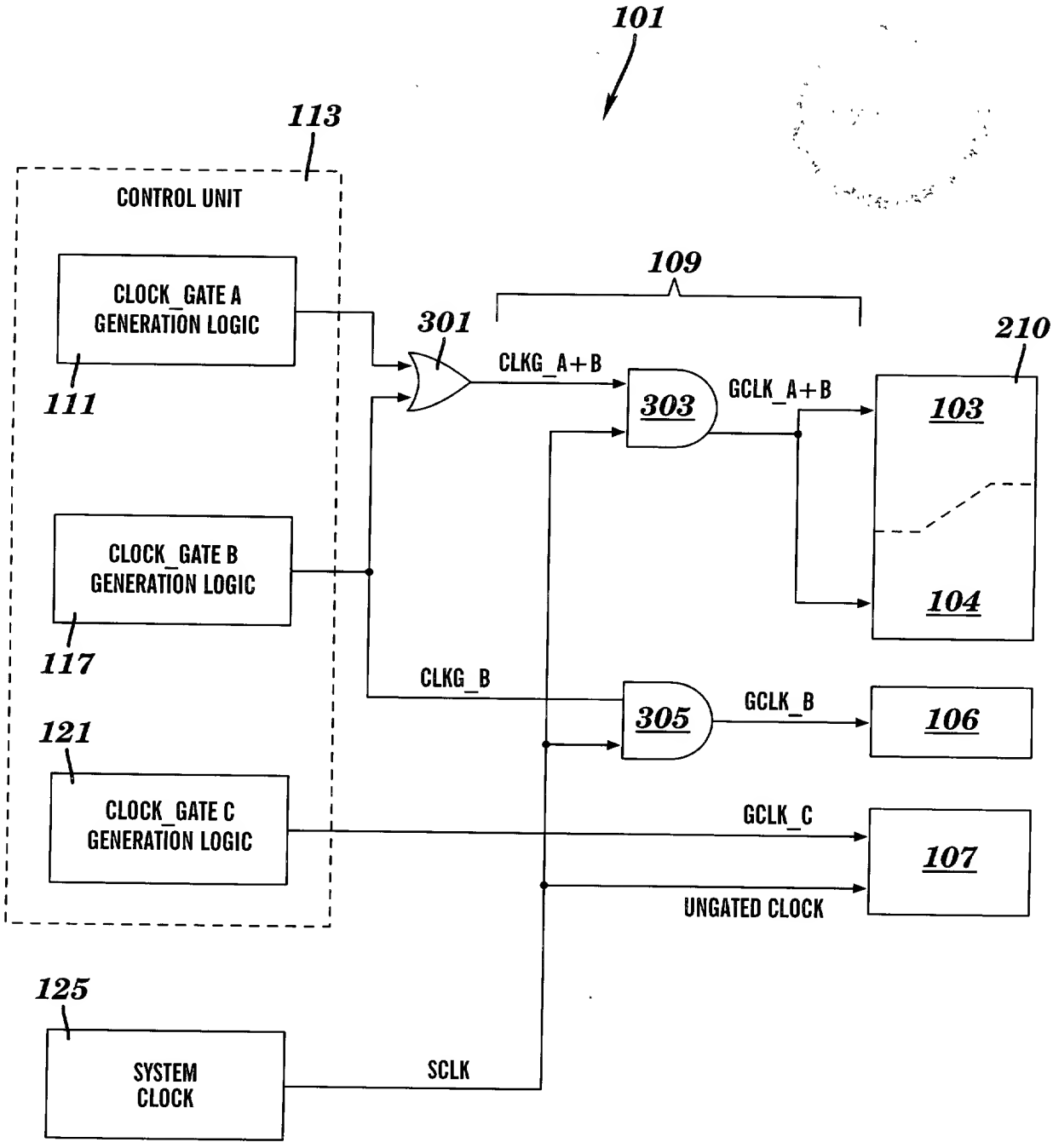

101
113
CONTROL UNIT
CLOCK_GATE A GENERATION LOGIC
111
CLOCK_GATE B GENERATION LOGIC
117
121
CLOCK_GATE C GENERATION LOGIC
125
SYSTEM CLOCK
SCLK
109
301
CLKG_A+B
303
GCLK_A+B
210
103
104
CLKG_B
305
GCLK_B
106
GCLK_C
107
UNGATED CLOCK

FIG. 3g

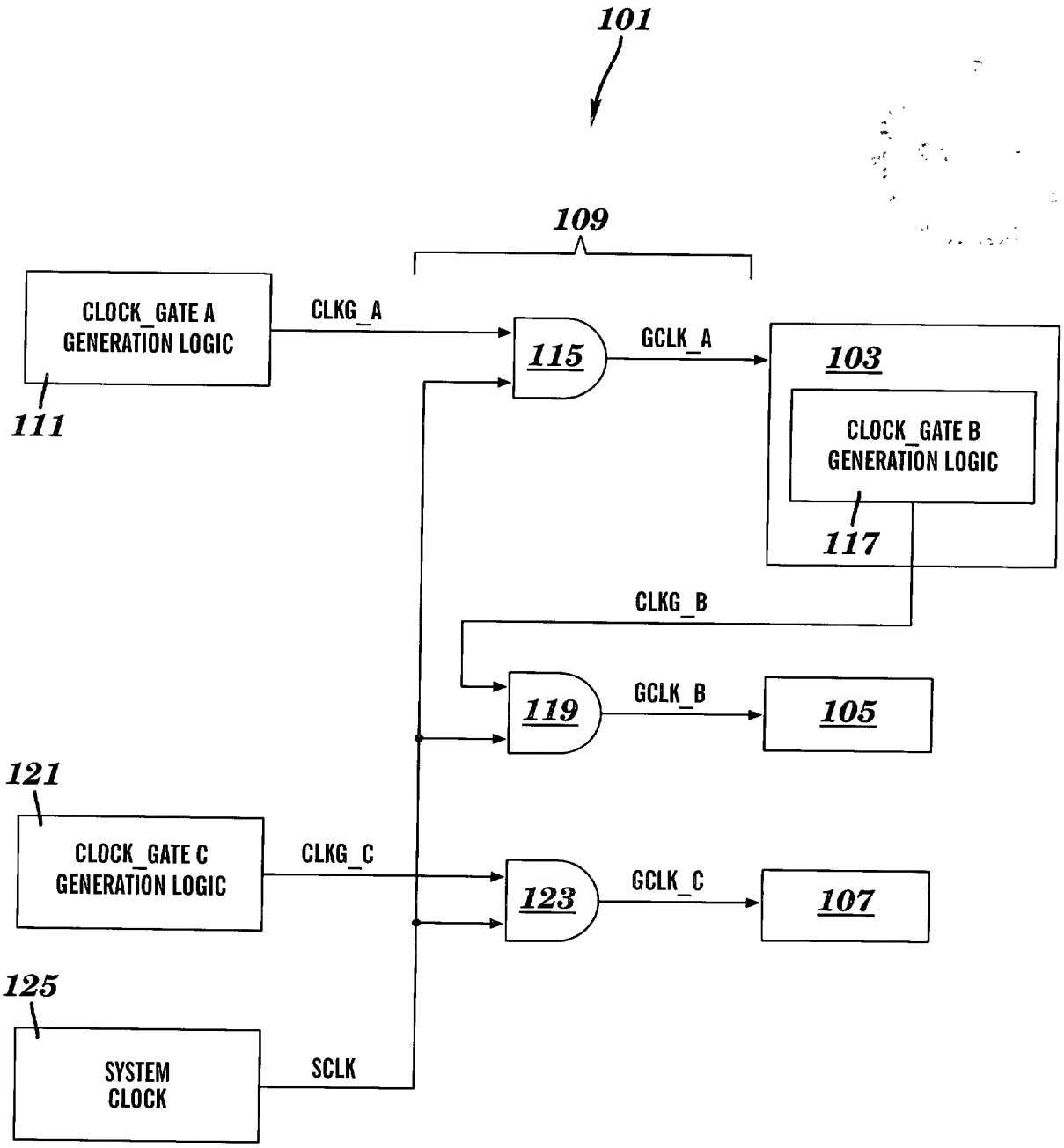

101
109
CLOCK_GATE A GENERATION LOGIC
111
CLKG_A
115
GCLK_A
103
CLOCK_GATE B GENERATION LOGIC
117
CLKG_B
119
GCLK_B
105
121
CLOCK_GATE C GENERATION LOGIC
CLKG_C
123
GCLK_C
107
125
SYSTEM CLOCK
SCLK

FIG. 3h

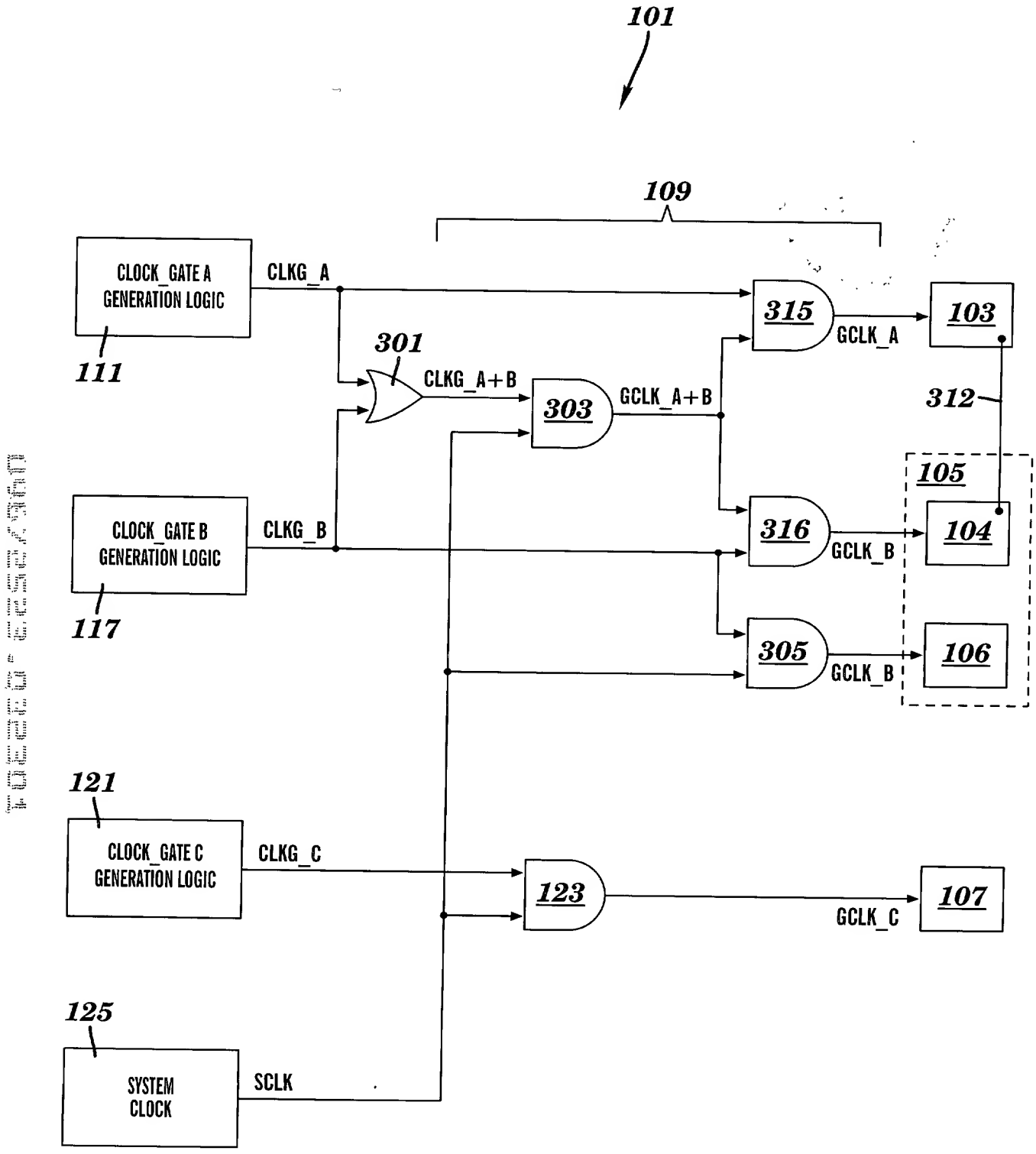

101
109
CLOCK_GATE A GENERATION LOGIC
111
CLKG_A
315
GCLK_A
103
301
CLKG_A+B
303
GCLK_A+B
312
105
CLOCK_GATE B GENERATION LOGIC
117
CLKG_B
316
GCLK_B
104
305
GCLK_B
106
121
CLOCK_GATE C GENERATION LOGIC
CLKG_C
123
GCLK_C
107
125
SYSTEM CLOCK
SCLK

FIG. 3i

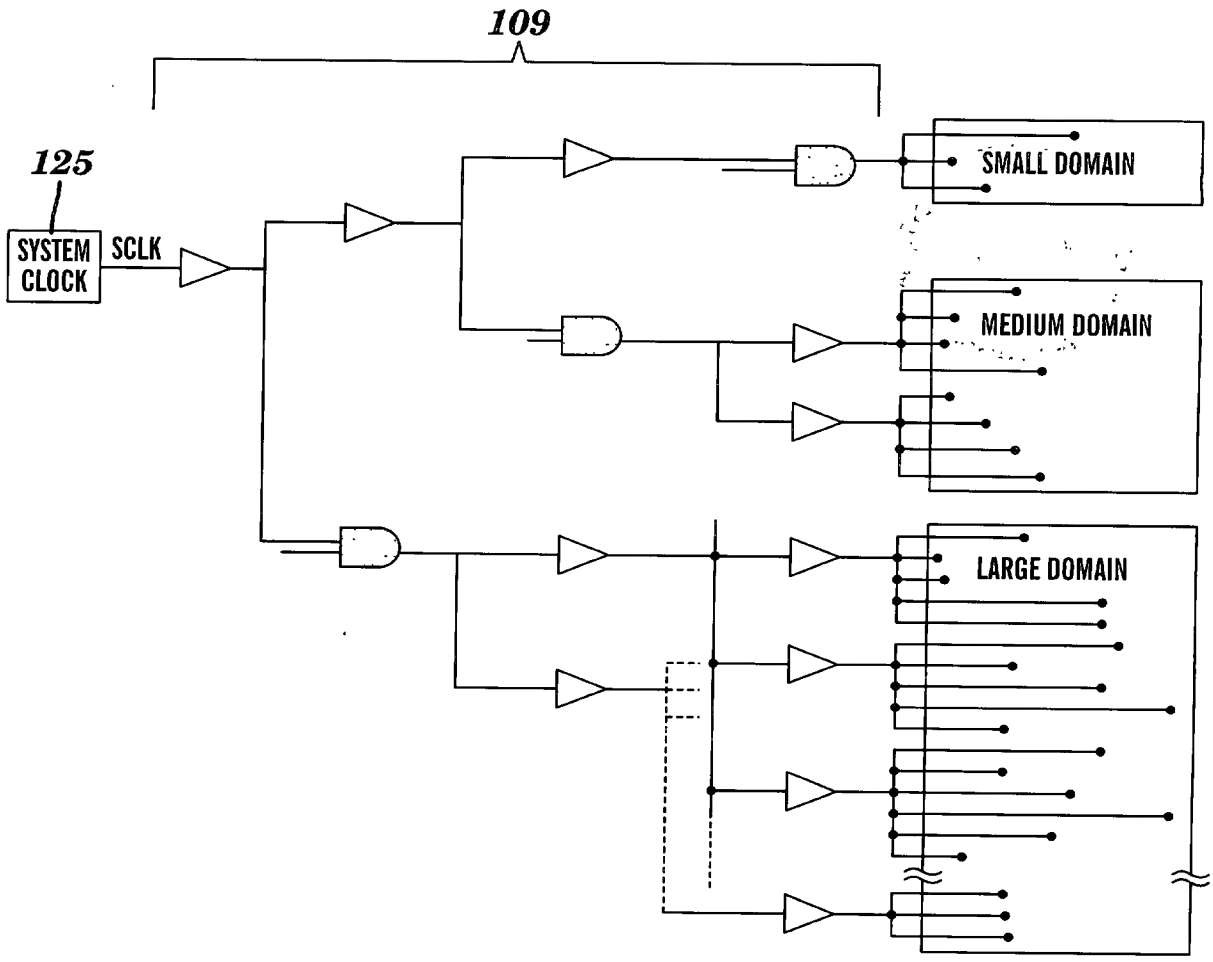

109
125
SYSTEM CLOCK
SCLK
SMALL DOMAIN
MEDIUM DOMAIN
LARGE DOMAIN

FIG. 2f

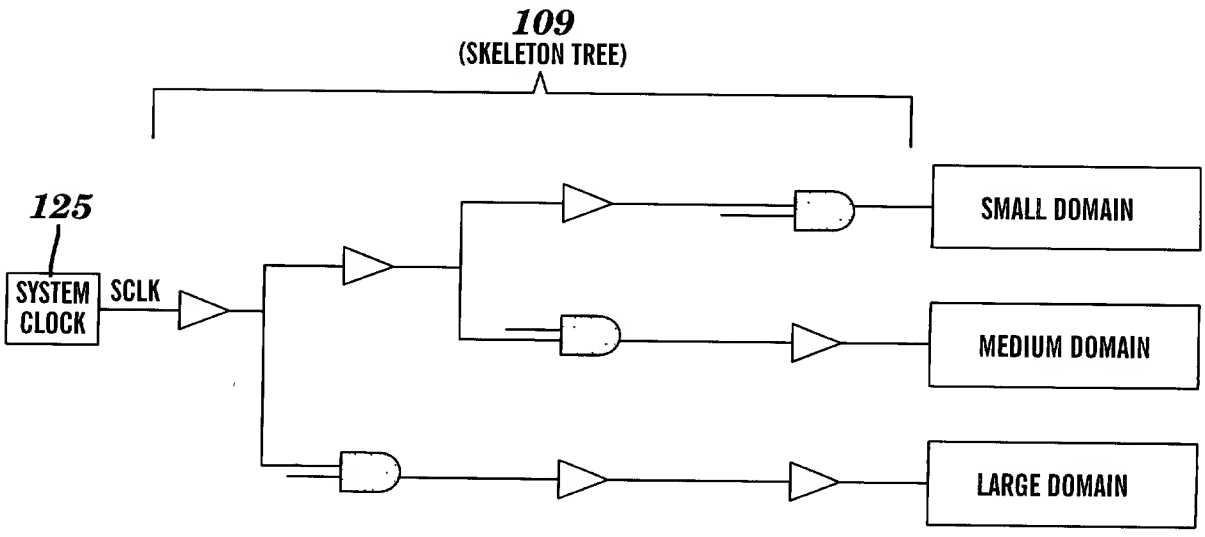

109
(SKELETON TREE)
125
SYSTEM CLOCK
SCLK
SMALL DOMAIN
MEDIUM DOMAIN
LARGE DOMAIN

FIG. 2g

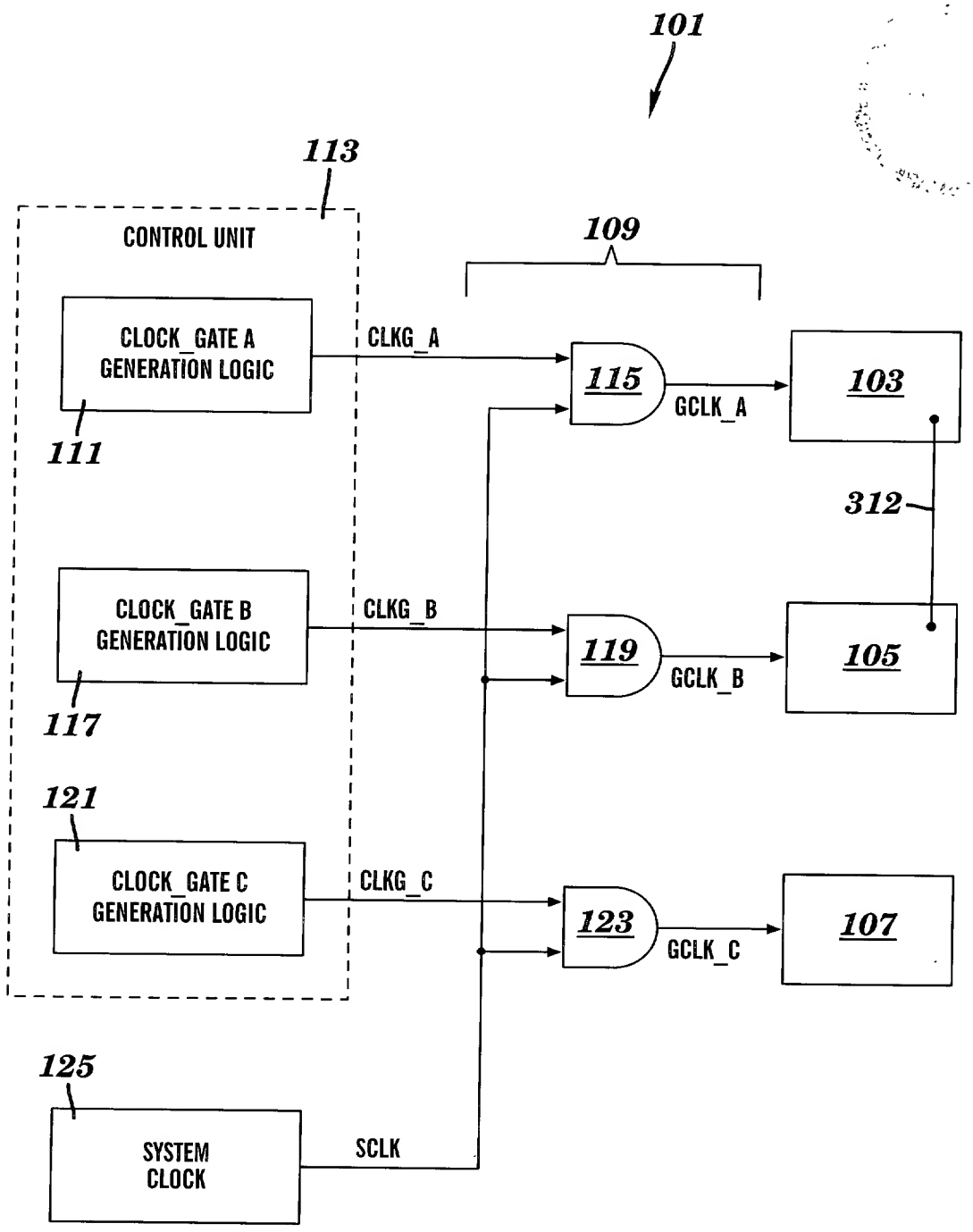

101
113
CONTROL UNIT
109
CLOCK_GATE A GENERATION LOGIC
CLKG_A
115
GCLK_A
103
111
312
CLOCK_GATE B GENERATION LOGIC
CLKG_B
119
GCLK_B
105
117
121
CLOCK_GATE C GENERATION LOGIC
CLKG_C
123
GCLK_C
107
125
SYSTEM CLOCK
SCLK

FIG. 3a